APPENDIX 4

A Description of Circuits for Determining & Stabilizing Frequency

The transmitter frequency is determined and stabilized by a PLL synthesizer based on a Frequency Synthesizer IC, LMX2332A (U12 on RU RF Board).

The LMX2332A employs a digital phase-lock loop technique. The reference oscillator is a 20.48MHz TCVCXO (X3 on the RU Baseband Board) that has inherent stability of +/- 2.5ppm over the temperature range –30 to +70 degrees Celsius. Frequency control is further improved by controlling the TCVCXO to an accuracy of better than 0.1ppm by reference to the pilot tone received on the downlink command channel from the Base Station. Frequency accuracy of the downlink command signal itself is controlled within 0.01ppm by the 40MHz OCXO reference oscillator in the Command Unit of the Base Station.

B Description of Circuits and Devices employed for Suppression of Spurious Radiation, for Limiting Modulation and for Limiting Power

Suppression of Spurious Radiation

A harmonic filter is employed between the Transmitter PA output and the antenna port to attenuate spurious radiation. This filter consists of C48, C37, L2, L22, C28, L1 and C27.
Synthesizer phase noise is minimized in the basic design and is further reduced by operating the PLL at 880MHz and then dividing by 4 to achieve the required 220MHz.
The PA itself is highly linear and is controlled by a Cartesian Loop linearizer.
The band plan for this 16QAM-modulation multi-channel narrow-band system requires a transmitter emission mask that provides –47dBc at +/-10kHz; this ensures excellent suppression of spurious radiation.
Additionally, an instability detector circuit monitors the spectral energy (about 200kHz above the carrier frequency) in the Cartesian loop and shuts down the transmitter in event of PA instability.

Limiting Modulation

A Cartesian Linearizer circuit is employed not only to provide linearization, but also to limit modulation.

> The software-derived baseband I and Q signals from the Baseband Board and the feedback I and Q signals from the Cartesian loop are combined in the summing operational amplifiers U13B and U13C. A subtraction process is performed in order to generate error signals, which are fed to the I/Q Modulator (U21), ensuring that the RF signal input to the amplifier stages is at the correct level.

Limiting Power

For limiting power, the gain of the final power amplifier is limited by zener diode Z1; this limits the bias voltage applied to the final power MOSFET Q17 and hence limits the quiescent current and the stage gain.