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LD/ECS/TB/GDC (Magnus Abrahamsson)	98-03-13 PA1	

~~Approved according to 1776 - 2/ROA 117 3750 -~~

TECHNICAL DESCRIPTION:

LOGIC AND AUDIO CIRCUITS

ON THE TRANSCEIVER BOARD

CONTENTS

1 GENERAL

This document describes the logic and the audio processing circuits which are part of the transceiver board mounted in dual mode digital pocket phones of AMPS - GSM type.

The other part of the transceiver board that carries the radio circuits is described in the corresponding document starting with 1/1551 -.

The primary purpose of the logic part is to control and monitor transmission and reception, to co-operate with the telephone exchanges of the mobile telephone system and to do the processing of audio signals to and from the mobile phone.

Chapter 2 contains information about document revisions.

In chapter 3 is the data flow through the phone described in both TX and RX direction.

In chapter 4 are several of the electrical functions and circuits described more in detail.

Chapter 5 describes the different memory types used in the phone.

In chapter 6 the layer structure of the PCB is briefly described.

1.1 CROSS REFERENCES

1.1.1 Names

In most cases the different circuits in the phone are given names which are used during the development phase. These names are also used in this description.

The following list shows the used circuit names and the corresponding position numbers used in the schematics.

JOHANNA	D600
EBBA	D900
PATTI	N800
FLASH	D610
EEPROM	D630

1.1.2 Abbreviations

Some common abbreviations are used in the text. These are explained below.

A/D	Analogue/Digital
CUI	Command User Interface
D/A	Digital/Analogue
DSP	Digital Signal Processor
HW	Hardware
LED	Light Emitting Diode
LCD	Liquid Crystal Display
MS	Mobile Station
PCB	Printed Circuit Board
PFET	P-channel Field Effect Transistor
PWM	Pulse Width Modulation
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
RTC	Real Time Clock
RX	Receive
SIM	Subscriber Identity Module
SMT	Smart Voltage
TX	Transmit

2 CHANGES BETWEEN REVISIONS

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3 DATA FLOW

A general block diagram for the GSM phone is shown in the figure below. It shows the data flow through the GSM phone. It also indicates the different hardware parts involved in the transmission.

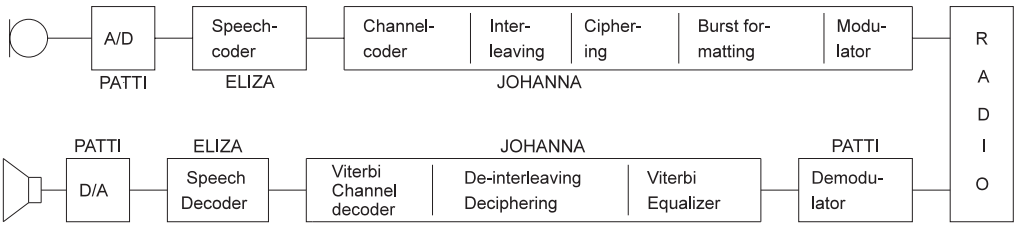

Figure 1 Block diagram for GSM phone.

All names in the middle of figure 1 correspond to the actual circuit that performs the indicated task.

JOHANNA controls the data flow. This is the central unit containing the microprocessor, Z80, RAM and the interfaces to external circuits and units, memories and the radio. It also performs a lot of the signal processing not done in the other circuits.

3.1 TX PATH

3.1.1 GSM Mode

The speech signal from the microphone is amplified and digitized to a 13 bit-PCM signal in PATTI. It is then sliced into 20 ms pieces and thereafter speech coded in EBBA to reduce the bit rate. Further data processing is carried out in JOHANNA which includes channel coding, interleaving, ciphering and burst formatting. The data is then put through a wave form generator (IQ signal) before it is fed to the radio.

The interleaving causes a small delay. Ciphering is done with a relationship of 1:1 (input: output) and then the bits are formatted into eight half bursts (for every 20 ms of speech). These are then transmitted in the proper time slot at a rate of about 270 kbit/s.

3.1.2 AMPS Mode

The speech signal from the microphone is amplified and digitized to a 13 bit-PCM signal in PATTI. It is then fed to the DSP EBBA where some signal processing including 2:1 compressing and preemphasing is performed. Finally an analogue waveform generator in JOHANNA produce the I and Q signal to the radio.

3.2 RX PATH

3.2.1 GSM Mode

The receiver path works as follows. The signals RXIFP and RXIFN from the radio are hard limited phase modulated and differential signals that contain all the data received. A fast phase digitizer in PATTI demodulates these signals. The phase information is then fed to JOHANNA together with A/D converted RSSI signals provided by the radio. The three RSSI signals are currents that in the first step are converted to a voltage and secondly A/D converted in PATTI.

The bursts received are then further processed in JOHANNA mainly in the same way as in the TX path but in reversed order and with reversed functions. That is deciphering, de-interleaving and channel decoding.

The first step in JOHANNA is however an equalizer that performs a Viterbi algorithm to create a channel model.

After all eight half bursts have been received and deciphered, they are reassembled into a 456 bit message. The sequence is decoded to detect and correct errors during the transmission. The decoder uses soft information (probability that a bit is true) from the equalizer to improve error correction.

Finally the bit stream is speech decoded in EBBA and then transformed back into analogue speech in PATTI.

3.2.2 AMPS Mode

The 450 kHz Intermediate Frequency (IF) from the radio is fed to an analogue comparator in JOHANNA which generates a digital IF signal to the Phase Digitizer. The Phase Digitizer calculates the relative phase and modulation frequency of the IF signal and the result is transferred to the DSP EBBA. In EBBA the audio information in the frequency is deemphased, expanded and converted to 13 bit PCM code which is sent to PATTI. Finally the bit stream is transformed back into analogue speech in PATTI.

4 DESCRIPTION OF VARIOUS FUNCTIONS

4.1 ON OFF CIRCUITRY

As long as the phone is turned off the enable input of the regulators are kept low by the pull down resistor. When the ON/OFF button is pressed the signal ONSRQ is connected to VBATT. When setting ONSRQ high it will set the REGON signal high via a diode. The REGON signal enables the regulators which will power up the regulators and the rest of the phone.

Among the very first actions from the program is to turn the DCON signal high and thus keeping the REGON signal in a high state. From this point the ON/OFF button can be released. JOHANNA will now keep control over the REGON signal through the signal DCON.

The MS is turned off by pressing the ON/OFF button again. This action doesn’t affect the state of the REGON signal, it’s already high due to the

DCON signal. The ONSRQ signal is also linked to the keyboard matrix through a transistor switch. JOHANNA senses the signal (ONOFF) and the program can turn off the MS by releasing the DCON signal in a controlled way.

4.1.1 Auto Turn On

The CPU will automatically switch on, if a charger is connected. The signal AUTOON from the charging circuit PIA-MIA in the Radio part will then generate the enable signal, REGON, to the regulators. AUTOON is gated to REGON via a switch transistor and is only used to turn the phone on. After turn on JOHANNA takes control of REGON.

4.1.2 Alarm

The phone is switched on at Alarm from the RTC. DCON will then be generated directly from the RTC block with no influence from the CPU, which has no power, until DCON has switched on the regulators.

4.2 POWER SUPPLY

There are two ways for the mobile to get power. If a battery is used, which is the common way, it is fed through two contacts on the PCB and then linked through the PCB to the regulators on the logic and radio part. The other way is through the system connector, see reference [1].
A battery must always be attached to get the phone powered up.

The VBATT line is switched through a PFET, which acts as a switch for the DCIO voltage and also as charge switch. The switch is controlled by PIA-MIA. See [2]

Different independently regulated regulators make up the voltages on the logic side.

The different voltages are:
VDIG/VANA used for JOHANNA logic pads, all the memories, LCD and for the mixed mode circuit PATTI.
VDSP is used for the DSP EBBA padring only. The reason is that the DSP works in a burst mode in short periods but with high current consumption.
VDSPC is used for the DSP core. This is mainly VDSP that is regulated by a single transistor. Lover voltage causes lower power consumption.
VRTC is used to supply the RTC block in JOHANNA. A small 3.5 V regulator provides this voltage with extremely low quiescent current. This voltage is always powered up when a battery is connected.
SIMVCC is controlled from the SIM interface in JOHANNA to save power and is used for the SIM interface.

VBATT is the unregulated battery voltage.

The voltage **VRPAD**, generated on the radio part, is used for the radio interface on JOHANNA and as a voltage reference for the generation of the top indicator LED signals.

An error flag output, PWRRST, which warns for low output voltage due to low battery voltage is generated by a reset circuit. The error flag output is an open collector type. If the VDIG voltage used on the radio part drops below than typical 2.8 V the signal PWRRST goes low. This will cause a HW reset to JOHANNA and the signal that keeps the station turned on, DCON, will go low and the MS is turned off.

The signal PWRRST is also, as the name may indicate, the power reset to JOHANNA at power up. An external RC net connected to the reset circuit gives a proper timing for the reset signal during power up.

4.3 AUDIO

Most of the audio processing is made in PATTI by the voice codec that converts between analogue speech signals and 13 bit linear PCM code in both RX and TX paths. PATTI also includes audio filters and amplifiers for microphone and earphone.

The microphone is connected differentially to PATTI. It is biased by a reference signal, CCO, from PATTI, which is properly filtered on the circuit board. In the microphone path is also a high pass filter designed in that will cut frequencies below approximately 300 Hz.

PATTI communicates with JOHANNA by means of a number of serial interfaces. Loading the D/A, settings and other control of PATTI is made on the serial link CNVxxx. Data from A/D converter and phase digitizer is received on the serial link RADxxx. The signals DAR 0-1 are used to quickly switch between four pre-loaded registers in the D/A converter. This is used to control the ramp up and down of the POWLEV signal.

4.4 BUZZER AND TOP INDICATOR

The buzzer is supplied with voltage directly from **VBATT** over a 10 Ω current limiting resistor. The sound pressure in the buzzer will drop as the battery voltage goes down. This can be SW-controlled by adjusting the duty cycle.

The buzzer is controlled from the TONGEN block in JOHANNA by the signal BUZZ. The current through the buzzer is switched by a transistor.

The top LED is supplied by **VRPAD**. Both top indicators, the red and green LED are directly driven by a port pin on JOHANNA, no external transistors are used.

4.5 KEYBOARD SCANNING

The keyboard scanning is performed by 9 signals connected to the PORT block in JOHANNA; KEYCOL 0-3 (open drain outputs) and KEYROW 0-4 (CMOS inputs with internal pull-ups). These signals are arranged in a matrix 4*5 and each cross point can provide the functionality of one key button. In standby, when no scanning is performed, all the outputs are held low and all inputs are at high level due to the pull-ups.

Whenever a user presses a key button, one of the inputs goes low and generates an interrupt. The software starts the key scanning procedure to determine which cross point was activated.

The maximum number of keys in a 4*5 matrix is 20. However it is possible to add more keys by connecting each of the inputs to ground.

4.6 KEYBOARD AND DISPLAY ILLUMINATION

The keyboard illumination is made up of six LEDs connected in parallel. The display illumination is made up of four side beam LEDs in parallel. The current to these branches is controlled by two transistors, one for the keyboard and one for the display illumination.

Both transistors share the control signal LED3K from JOHANNA. The signal passes a resistor divider. This will provide a fairly constant voltage (1.75 V) on the transistor bases which controls the current through the transistors to a specific level (constant current generator). By two low valued resistors in the collectors branch for each transistors, the current and thus the brightness of the keypad and display illumination can be tuned independently to a suitable level.

4.7 LCD VOLTAGE REGULATION

For best performance concerning viewing angle and contrast ratio, the VLCD voltage to the LCD has to be regulated quite accurately by the logic. The signals PWM0 and PWM1 from JOHANNA are digital CMOS signals which mark/space ratio can be controlled by software. Both are implemented in HW, but only PWM0 is used in this application.
When the digital pulses pass a capacitor, the positive overshoots are shorted to ground and the negative will discharge the capacitor on the charge pump output. The voltage over this capacitor is decreased and generates the negative voltage, VLCD.

The voltage of VLCD is highly dependent of the load. To reduce the voltage variation for different loads, the VLCD voltage is passed to an A/D input on PATTI through a voltage divider. This input is then checked by software and regulated to match values given in a table. This means that VLCD can be temperature compensated.

4.8 REAL TIME CLOCK

The real time clock is a part of the JOHANNA chip. A 32.768 kHz crystal is placed close to the inputs on JOHANNA. The RTC is powered by a separate voltage, VRTC.

The RTC is always powered as long as the main battery is connected. On the output of the regulator is a backup capacitor connected. This capacitor will give power enough to keep the RTC alive at least 24 hours after the main battery has been disconnected.

The backup capacitor is a coin type rated 2.5 V and 0.3 F. The ground connection is a voltage divider to ensure that the maximum voltage over the capacitor never exceeds 2.5 V.

5 MEMORIES

Three different memories are used on the logic board: RAM, EEPROM and FLASH memory. The RAM is integrated in the Johanna chip. FLASH is connected to the common address and data bus. For control the signals WE, ROMOE and ROMCS are used. The EEPROM is connected to the I^2C interface on JOHANNA, a two wire serial link that is shared with the LCD driver.

5.1 FLASH

The FLASH memory is a block architecture memory which includes block selective erasures, automated write and erase operations. The memory is organized as 1024k*8 and is divided into separately erasable blocks. We don’t use the block architecture in our application, the memory is regarded as one continuos memory.

Program and erase operation is performed by communicating with the internal CUI. An internal write state machine automatically executes the algorithms and timings necessary for program and erase operations.

The VPPFLASH is connected to pin VPP on the device. To erase and program the memory, VPPFLASH must be at minimum 11.4 V and maximum 12.6 V. The nominal voltage of VPPFLASH is 12.0 V.

Some second source suppliers of FLASH memories do not require 12 V programming voltage. Applying 12 V VPPFLASH to these memories does not harm them.

5.1.1 Programming

It is possible to use FLASH memories and perform on board programming. The erasing and programming of the FLASH is then completely software controlled. The software communicates with an external equipment through a serial link. During erasing and programming the software runs in RAM.

To perform programming of the FLASH, a special hardlock together with the loader SW is needed.

To perform erasing and programming, VPP must be supplied. VPP is applied to the system connector on the terminal VPPFLASH. This pin is also used to disable the watchdog function in JOHANNA.

The procedure to load a program for the first time in the production line is as follows:

When the phone is powered up and the signal PWRRST is released the software starts to read the first instruction in the flash memory (after a short delay). Now, if the SERVICEI signal is activated, the very first instruction is read from an internal ROM in JOHANNA. This is a small ROM containing a very simple ”boot strap loader”. The actions of this code is to listen to a specific code on the serial link, TTMS. This indicates that the user wishes to download another program called the “hexloader” to the RAM. If this code is not received within 2 seconds the execution is automatically switched over to continue in the FLASH.

If the “hexloader” is successfully loaded into RAM the execution starts in RAM. With help of the “hexloader” it is now possible to execute the algorithm to download and program any code received on TTMS. It is also possible to erase the FLASH or to read the manufactures device code of that particular flash memory.

5.2 EEPROM

The EEPROM density is 16k*8. This memory is interfaced by a two wire serial bus, I^2C. All read and write operations are performed through this serial bus.

6 PRINTED CIRCUIT BOARD

The printed circuit board is a 6-layer board. Layer 1,2 & 6 carry most of the connections between component terminals. Layer 3 & 5 constitutes of ground planes, DGND, and covers the whole board. Layer 4 is mainly ground but with some Strip lines in the radio part.

No layer is made up to carry the different voltage planes VDIG, VDSP, VANA and the VBATT signal. These signals are though wider because they must be able to carry a lot of current.

The layer structure is listed below:

Layer 1	Components, signals (Primary side)
Layer 2	Signals
Layer 3	Ground plane
Layer 4	Ground plane with Strip lines
Layer 5	Ground plane
Layer 6	Components, signals (Secondary side)

7 REFERENCES

[1] Description of fundamental interfaces from the *"4 volt"* product platforms, CX/B 95:0202.

[2] Technical description radio on transceiver board, 1/1551 - ROA 117 3313.

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TECHNICAL DESCRIPTION:
RADIO CIRCUITS ON TRANSCEIVER BOARD ROA 117 3750

1 GENERAL

This document describes the radio circuits which are a part of the transceiver board mounted in a PCS/AMPS pocket phone. The phone is able to operate in the GSM 1900 and AMPS 800 band.

The other part of the transceiver board, which carries the logic and audio circuits, is described in the corresponding document 2/1551-ROA 117 3750.

The primary purpose of the radio part is in the receiving mode to convert the wanted information from the adjusted radio frequency to base band signals which are handled by the logic circuits. In the transmitting mode the phone is converting the information carried by the base band signals (provided by the logic part) to a certain radio frequency channel in the wanted band.

2 CHANGES BETWEEN REVISIONS

3 INTERACTION

The radio interacts with different parts of the phone. These parts are the logic circuits via the radio-logic interface, the antenna or external antenna via antenna connector and battery via the battery connectors.

There are testpoints to measure some specific signals in the radio circuits.

The radio has a complete shield surrounding it in order to avoid unwanted radio interaction with surrounding fields. This shield consists of a metal frame, conducting gaskets and completely metallized bottom surface of key board.

4 FUNCTION

4.1 BLOCK DIAGRAM

A general block diagram for the radio part of the PCS/AMPS telephone is shown below (Fig.1). The radio is designed to select the wanted channel and convert that RF signal to a signal which can be handled by the logic. This has to be done without transmitting spuriouses disturbing other radio traffic and fulfilling the requirements in presence of disturbing RF signals. In order to minimize current consumption all parts in the radio are only powered up during the needed timeslot. There are several signals from the logic controlling the radio and its frequency generators. Radio and logic are mounted on the same PCB but have separate shielded cavities in order to avoid unwanted disturbances.

There is an antenna switch for the PCS band. The band selection is accomplished by software control. Only one band can be activated at a time. The switch are used to select the connection of either the PCS receiver or the PCS transmitter to the antenna in PCS mode. In AMPS, both receiver and transmitter are activated at the same time in conversation mode. No RF switches are used in AMPS mode.
A separate mechanical switch in the antenna connector selects if the normal antenna or an external antenna shall be used. It is only the connector for external antenna (on the back of the phone) that is 50Ω.

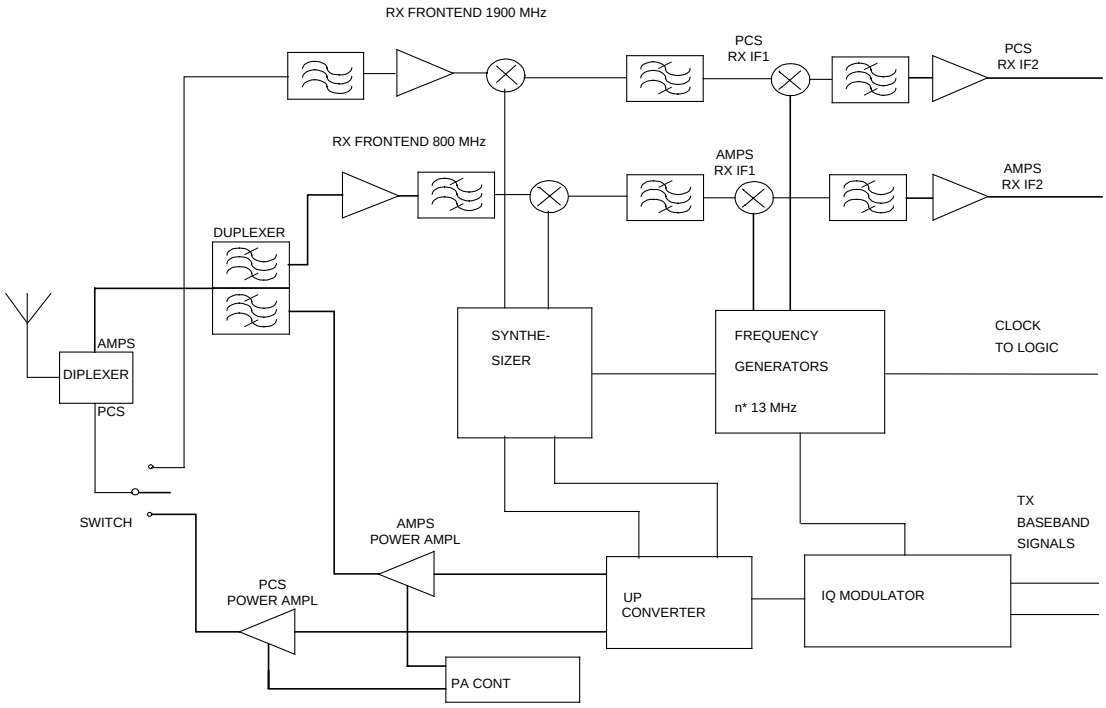

Fig. 1

4.2 RX-FRONTENDS

The frontends are filtering out the AMPS receive band 869-894MHz respectively the PCS (GSM 1900) receive band 1930-1990 MHz. Amplification of the complete band is performed and downmixing of the wanted channel to the first fixed IF frequency at 72 MHz for AMPS and 188 MHz for PCS. The frontend section consists of one common high frequency RF-ASIC circuit. Filtering is done with a duplex filter in the 900 MHz band and a ceramic filter in the 1900 MHz band.

4.3 RX-IF

The IF signal is amplified, filtered and converted to a second IF of 450 kHz in AMPS and 6 MHz in PCS before being feed to the AD-converter. The RX-IF parts consists of two different RF-ASICs. One for each band. The channel filtering is distributed over several filters in SAW and ceramic technologies.

4.4 TX-IF

The TX IF starts with an IQ modulator that upconverts the baseband I and Q signals coming from the DA converter. The IQ modulator works on an IF frequency. This IF signal is then bandpass filtered. The TX-IF circuitry is implemented in an RF-ASIC. A frequency upconverter circuit is moving then the information to the wanted channel in the 824-849 MHz band or to the 1850-1910 MHz band.

4.5 POWER AMPLIFIER

There are different PA-ICs. One for each band. The signal from the upconverter circuit has a low fixed amplitude and is fed to the active PA. To fulfil the PCS spectrum requirements it is also necessary to ramp up/down to the wanted level in a controlled way. This is done in an integrated power amplifier together with a control loop. The output of the PCS PA is connected to the antenna switch and the output of the AMPS PA is fed to the TX port of the duplexer. Filters are provided in these lines to suppress unwanted spurious signals.

4.6 FREQUENCY GENERATORS

A voltage controlled crystal oscillator at 13 MHz is the frequency base for the complete transmitter. The frequency of this oscillator is locked to the received frequency in order to achieve the 0.1 ppm requirement in the GSM specification.

This 13 MHz signal is buffered and used both by the logic as system clock and by the radio as reference in local oscillators.

The main synthesiser is able to operate as a local oscillator for the 900 MHz as well as for the 1800 MHz band. The main synthesizer has the dual function of downconverting the wanted RX channel to RX-IF and to downconvert the TX-signal to the TX-IF, which is necessary for the upconverting loop. It is a fractional-N synthesizer working with the channel distance, 200 kHz or 30kHz as reference.

The upconverter consists of two oscillators (one for each band) which are controlled by a signal provided by the IF RF-ASIC. These oscillators are operating directly in the transmit bands. Channel selection is accomplished by the main synthesiser.

In the IF section for PCS, there is a local oscillator acting as a downconverting LO in the RX-mode and as an upconverting LO in the TX-mode. The frequency is adjusted individually for each mode. In AMPS mode there is an standard synthesizer, creating a 2:nd LO signal for the receiver.

4.7 POWER SUPPLY

Three linear regulators are used with an output voltage of 3.8 V. Some circuits like the power amplifier are directly connected to the battery.

5 INTERFACE RADIO-LOGIC

The radio is connected to the logic part by 34 signal lines. All these signal lines are running internally on the PCB. There are test pins on some of these connections which makes it possible to check the functionality. It is however not possible to control the radio without using the logic on the transceiver board.

List of radio - logic connections.

Signal	Name	Function	Origin
1	SYNSTR	Synth Programming, strobe	Logic
2	SYNCLK	Synth Programming, clock	Logic
3	SYNDAT	Synth Programming, data	Logic
4	RFACLK	RF ASIC programming, clock	Logic
5	RFADAT	RF ASIC programming, data	Logic
6	RFAENB	RF ASIC programming, enable	Logic
7	SYNTON	Synth On/Off	Logic
8	VCXOCONT	VCVCXO , frequency control	Logic
9	TXVCO	TX VCO, frequency preset	Logic
10	POWLEV	Power amplifier, power control	Logic
11	TEMP	Temperature sensor	Radio
12	MCLK	13 MHz system clock logic	Radio
13	RSSI1	Received Signal Strength 1	Radio
14	RSSI2	Received Signal Strength 2	Radio
15	RSSI3	Received Signal Strength 3	Radio
16	RXIFP	Hard limited 6 MHz IF	Radio
17	RXIFN	Hard limited 6 MHz IF	Radio
18	MODIP	TX base band I signal	Logic

19	MODIN	TX base band I signal	Logic
20	MODQP	TX base band Q signal	Logic
21	MODQN	TX base band Q signal	Logic
22	RXON	RX circuits On/Off	Logic
23	TXON	TX circuits On/Off	Logic
24	ANTSW	Antenna Switch RX/TX	Logic
25	DCIO	Battery charge supply/accessory supply	Logic/Radio
26	VBATT	Battery voltage	Radio
27	VRPAD	Regulated voltage for interface, digital ASIC - radio	Radio
28	REGON	General radio switch On/Off	Logic
29	SWDC	Switched battery voltage	Radio
30	IMEAS	Battery charge current sensor	Radio
31	VTRACK	Battery voltage sensor	Radio
32	ICONT	Battery charge current control	Logic
33	AUTOON	Detect signal for battery and charger	Radio
34	BAND_ MODE_SEL	Band switching signal	Logic
35	RSSI_AMPS	Received Signal Strength for AMPS	Radio
36	RXIF_AMPS_N	Hard limited 450 kHz IF	Radio
37	RXIF_AMPS_N	Hard limited 450 kHz IF	Radio

6 REFERENCES

Technical description Logic and Audio Circuits On Transceiver Board 2/1551-ROA 117 3750.

DESCRIPTION

2.983 (c) This cellular transceiver is being prepared for quantity production.

(d) This transmitter is a microcomputer controlled synthesized transmitter operating in the frequency band of AMPS 824-849 MHz and GSM 1850-1910 MHz, Part 22H and Part 24 respectively. In the AMPS mode the frequencies are generated using a phase locked loop frequency synthesizer. The transmit audio contains a 2:1 ratio compander, 6dB/Octave pre-emphasis, ± 12 KHz deviation limiting and a post limiter filter per 22.907 (a).

In the GSM mode the transmitter is designed for use in a TDMA (Time Division Multiple Access) system. It is a constant envelope transmitter using GMSK 0.3 modulation. All audio processing is done by a DSP (Digital Signal Processor). There are 299 channels available with a channel spacing for 200kHz. For each channel there are 8 timeslots available.

(1) Type of Emissions:

800 MHz	AMPS	40K0F1D, 40K0F8W
1900 MHz:	GSM	255KGXW

(2) Frequency Range: 824-849 MHz AMPS
1850-1910 MHz GSM

(3) Range of Operating Power: This transmitter is designed for AMPS/GSM cellular mobile telephone operation. In the AMPS mode the transmitter is adjusted to achieve 0.4 watts measured at the antenna connector. The transmitter output is controlled by a binary data message emitted by the base station. The power level can be controlled in six levels each of 4 dB increments. Each power level will be maintained to +2, -4 dB over a temperature range of –30 to +60°C and a supply voltage, measured at the radio between 4.2 and 6.0 VDC.

When operating in GSM mode the transmitter is adjusted for a max1.0 Watt peak power, measured at the antenna connector. The output power is controlled by a binary data message emitted by the base station. The output power can be controlled in 16 levels, each of 2 dB increment. The power levels are labeled 0 through 15, where power level 0 is the highest output power, 1 Watt. Power level 0 will be maintained to ±2.5 dB over a temperature range of –20 to +60° C, and supply voltage, measured at the ±2, radio, between 4.3 and 6.5 Volts. Power level 1 through 8 will be maintained to ± 4 dB,. Power level 9 through 13 to ±5 dB and power level 14 and 15 to ±6 dB, in this temperature and voltage range.

(4) Maximum Power Rating: The maximum power rating under environmental and supply voltage variations when operating in an AMPS mode is equal to 0.5 watts ERP plus the power level tolerance of +2, -4 dB. Therefore the maximum output power is 0.95 watts ERP.

The maximum power rating under environmental and supply voltage variations when operating in a GSM mode is equal to 1.0 Watt EIRP plus the power level tolerance of ±2.5 dB. Therefore the maximum output power is 1.8 watts. This is the peak power in each burst. Since the transmitter is only operated with 1/8 duty cycle the maximum average power is 225 mW.

(4) DC Voltage and Current:

When operating in an AMPS mode the DC voltage and total input current of the entire final power amplifier module is +4.8 VDC and 300 mA in the highest level (0.4watts) to 30 mA in the lowest power level (0.006 watts).

When operating in a GSM 1900 mode the DC voltage and total input current of the entire final power amplifier module is 4.8 VDC and 1400 mA in the highest level (1.0 watts) to 300 mA in the lowest power level (0.001 watts).

EXHIBIT 12A3

GSM 1900 ALIGNMENT PROCEDURE

When operating in a GSM 1900 mode:

PARA. 2.983(d)(9)
Alignment Procedures

This specification describes the alignment done on the GSM 1900 transceiver during assembly and final test. All alignment is done using software communicating with DACs in the radio. Therefore, there are no mechanical adjustments to be made to the radio. Tuning data for transmitter power level etc.. is stored internally to the transceiver in an EEPROM.

RADIO TUNE/TEST INSTRUCTIONS

The FLASH memory must have been programmed with the operating software before beginning this procedure. Initial personality programming should have been done also at board flash. Operation of the radio during this procedure will be done using test mode software.

1900 MHz FILTERING

SAW and fixed ceramic elements, therefore no tuning is required at 1900 MHz.

BATTERY VOLTAGE CALIBRATION

A DC supply is connected to the transceiver. Internally to the radio there is a A/D converter sensing the DC voltage. The DC voltage is set to 4.5 V and 6.5 V and the corresponding readings from the ADC are stored in the EEPROM. The ADC is linear, meaning that the complete DC voltage range can now be measured.

REFERENCE FREQUENCY ADJUSTMENT

The Voltage Controlled Crystal Oscillator (VCXO) is tuned at the factory, and adjusted in the field under software control. In the field the TCXO is adjusted for minimal frequency error by the use of a software AFC algorithm. This algorithm locks the TCXO frequency to the received base station signal. There are also software algorithms that compensate for the aging and temperature drifts of the crystal. The voltage that controls the frequency is generated by a D/A converter. The value that is sent to the D/A converter to generate the proper voltage is determined at the factory and is stored in a non-volatile memory.

GSM 1900 ALIGNMENT PROCEDURE

PARA. 2.983(d)(9)
Alignment Procedures

TRANSMIT OUTPUT POWER CALIBRATION

For each of the transmitter output power levels 0 through 15 the DAC controlling the power is adjusted until the output power is within, 0.5 dB for power levels 0 to 7, and 0.7 dB for power levels 8 to 13, and 1.0 dB for power levels 14 and 15. The DAC settings are stored in a table in the EEPROM.

POWER TABLE SETTINGS

POWER LEVEL	POWER SETTING	TOLERANCE
0	30 dBm (1000mW)	+/- 2.5 dB
1	28 dBm	+/- 4 dB
2	26 dBm	+/- 4 dB
3	24 dBm	+/- 4 dB
4	22 dBm	+/- 4 dB
5	20 dBm	+/- 4 dB
6	18 dBm	+/- 4 dB
7	16 dBm	+/- 4 dB
8	14 dBm	+/- 4 dB
9	12 dBm	+/- 5 dB
10	10 dBm	+/- 5 dB
11	8 dBm	+/- 5 dB
12	6 dBm	+/- 5 dB
13	4 dBm	+/- 5 dB
14	2 dBm	+/- 6 dB
15	0 dBm	+/- 6 dB

RSSI (Receiver Signal Strength Indicator) CALIBRATION

The antenna input power is swept from –110 dBm to –40 dBm and the RSSI indicator current is read from the ADC. The corresponding digital values are stored in a table in the EEPROM.

GSM 1900 ALIGNMENT PROCEDURE

PARA. 2.983

RECEIVER ALIGNMENT

NO ALIGNMENT REQUIRED

AMPS ALIGNMENT PROCEDURE

When operating in an AMPS mode:

Alignment Procedure **Para. 2.983 (d)(9)**

GENERAL: All alignments, both in AMPS mode as well as in GSM 1900 mode, are done using a separate test software that is NOT incorporated in the phone when delivered to the end customer.

1.0 RADIO TUNE/TEST INSTRUCTION

1.1 800 MHz Filtering

All 800 MHz filtering is purchased ceramic elements, saw and monolithic elements, therefore no tuning is required at 800 MHz.

1.2 RF REFERENCE FREQUENCY ADJUSTMENT

This alignment is done in GSM 1900 mode.

1.3 TRANSMITTER ALIGNMENT AND TEST

The transmitter will always be on, no modulation, power level 2, and set to within ±5 channels of the center of the band unless otherwise indicated.

1.3.1 RF POWER

For each of the transmitter output power levels 2 through 7 the DAC controlling the power is adjusted until the output power is within, 0.5 dB. The DAC settings are stored in a table in the EEPROM.

POWER TABLE SETTINGS

POWER LEVEL	POWER SETTING
2	26 dBm
3	24 dBm
4	20 dBm
5	16 dBm
6	12 dBm
7	8 dBm

1.3.1 VOICE DEVIATION

The voice deviation is determined by DSP software settings and does not need to be aligned in production. Verification measurements are done in the factory.

1.3.1 VOICE DEVIATION (cont)

Modulation Monitor Settings: 50Hz LPF, 750 µS de-emphasis
C-Message Filter

Unmute audio, and Set the power level to PL 2. Apply a 2 V, 1.0 kHz tone to J602 pin 2. Verify that the measured frequency deviation is less than 12.0 kHz. Apply a 30 mVrms, 1 kHz tone to J602 pin 2. Verify that the deviations is 2.9 ± 0.29 kHz.

1.3.2 DTMF DEVIATION

The DTMF deviation is determined by DSP software settings and does not need to be aligned in production. Verification measurements are done in the factory.

Modulation Monitor Settings: 50 Hz HPF, 15 kHz LPF, no de-emphasis.
Set the radio to a midband channel and the power level to PL 2, and key the transmitter . Activate DTMF tone. Verify that the deviation is 6.6 kHz ± 10.

1.3.3 DATA DEVIATION

The DATA deviation is determined by DSP software settings and does not need to be aligned in production. Verification measurements are done in the factory.

Modulation monitory setting: 50 Hz HPF, > 20KHz LPF, no de-emphasis

With only the data path enabled and ST enabled, verify that the frequency deviation is 8.0 ± 0.8 kHz.

SAT DEVIATION

The SAT deviation is determined by DSP software settings and does not need to be aligned in production. Verification measurements are done in the factory.

Modulation Monitor Setting: 50 Hz HPF, > 20KHz LPF, no de-emphasis

Input a –30 dB signal to the antenna connector X101 on the selected midband channel, and modulate the generator with a 6K ±6 Hz sine wave at 2 kHz deviation. Turn SAT on, and verify that the frequency deviation is 2.0 ± 0.2 kHz.

1.4 RECEIVER ALIGNMENT

Turn the transmitter off, and set the synthesizer to within 5 channels of the center of the band unless otherwise indicated. Apply an ON-channel signal generator to the antenna connector X101.

1.4.1 AUDIO OUTPUT LEVEL

The Audio level is determined by DSP software settings and does not need to be aligned in production. Verification measurements are done in the factory

Signal Generator Setting: -50dBm at X101,1kHz tone at ± 2.9 kHz deviation.

Measure the audio voltage level at J602 pin 1, and verify that the level is 65 mV ± 10% at max. Volume level.

AMPS ALIGNMENT PROCEDURE

RECEIVER SINAD

Connect a device capable of measuring SINAD with C-message weighting to the audio output J602 pin 1.

Signal Generator Setting 870.03 MHz, -116 dBm at X101, 1kHz tone at ± 8.0 kHz deviation.

Set the radio to channel 001 and Verify that the SINAD is greater than 12 dB.

Circuit & Device Descriptions Para. 2.983 (d)(10-12)

Frequency stabilization circuitry and devices (2.983 d 10):

A voltage controlled temperature compensated crystal oscillator (VCTCXO) provides a reference frequency signal for the transmitter and receiver frequency synthesizers. It has a temperature stability of ± 2.5 ppm over the temperature range of –30C to +60C due to software temperature compensation. The VCTCXO is tuned at the factory, and should need no adjustment. The voltage that controls the nominal frequency is generated by two D/A converters. The values that are sent to the D/A converters to generate the proper voltages are set at the factory, but will automatically be adjusted by the temperature compensating algorithm, an aging algorithm and an AFC algorithm if necessary.

Attenuation of Spurious Emissions (2.983) (d) (11a)

Direct synthesis of the transmitter signal rather than frequency multiplication techniques ensure a spurious free spectrum of the transceiver. The only spurious signals are transmitter harmonics, reference oscillator 13 MHz with its harmonics, the local oscillators and the microprocessor clock.

The use of multi-layer printed circuit board, with signal tracks between ground planes reduces the radiation of any signal to a minimum. SAW bandpass filters for the duplexer attenuate conducted transmitter harmonics, reference oscillator and local oscillator signals. A bandpass filter in the receiver front end attenuates the local oscillator signal further. Additional suppression of radiation is achieved by shielding

Limiting Modulation (2.983 d 11b)

The modulator of the transmitter is proceeded by an ASIC which , together with the DSP, performs all audio processing functions including compression, pre-emphasis, limiting, and filtering. These devices provide an instantaneous control of the modulation waveform. An internal deviation adjustment stage, controlled by the SW, allows the maximum audio deviation to be set to ± 12 kHz.

Attenuation Higher Audio Frequencies

The limiting amplifier in the audio processing ASIC is followed by an internal low pass filter which provides an attenuation above 3 kHz in excess of that specified in 22.907(a). Manchester data signals are filtered prior to transmission by an internal low pass filter having an attenuation of 24 dB/octave above 20 kHz.

Output Power Control (2.983 d 11c):

A loop circuit under the supervision of the microprocessor sets the output power to any of six power levels.

By adjusting the DC bias of the power amplifier module, the output power can be controlled. This bias is the output voltage of an operational amplifier which compares the desired voltage from the logic section with a voltage derived from the instantaneous current consumption of the power amplifier . The loop forces the two voltages to be equal and , hence, the output power is regulated to any desired power level. Output power is stored in a digital memory. A lock detect signal from the synthesizer is fed to a circuit external to the microprocessor that prevents the transceiver from false transmission.

Para. 2.983 (d)(10-12)

Digital Modulation Techniques (2.983 d 12):

The 5K baud data stream is transformed to 10 kilobit/second Manchester encoded data in such a way that each NRZ binary one is transformed to a one-to-zero transition.

The Manchester encoded data stream is filtered before being applied to the modulator. Direct binary frequency shift keying is used. A binary one into the modulator corresponds to a nominal peak frequency deviation 8 kHz above carrier frequency and zero corresponds to a nominal peak frequency deviation 8 kHz below the carrier frequency.

GSM 1900 CIRCUIT & DEVICE DESCRIPTIONS

PARA. 2.983 (d)(10-12)

See attached document titled,	Technical Description: Logic and Audio Circuits on the Transceiver Board 2-1551 / ROA 117 3750 Uen Referenced Exhibit 12
See attached document titled,	Technical Description: Radio on Transceiver Board 1-1551 / ROA 117 3750 Uen Referenced Exhibit 12