SECTION 6 CIRCUIT DESCRIPTION

6.1 RECEIVER

6.1.1 INTRODUCTION

The receiver is a double conversion type with intermediate frequencies of 52.95 MHz and 450 kHz. The first injection frequency is phase locked to a temperature compensated crystal oscillator (TCXO) with a frequency stability of ±1.0 PPM from -30° to +60° C (-22° to +140° F). Two 3-pole bandpass filters in the front-end reject signals outside the receive band. Two 4-pole crystal filters and one 6-pole ceramic filter establish receiver selectivity (see block diagram Figure 6-1).

6.1.2 REGULATED VOLTAGE SUPPLIES

The +15V DC power source is supplied by the repeater power supply. The +15V supply enters the receiver on J201, pin 1. U206 provides the +12V DC receive voltage to the RF and IF amplifiers. U210 supplies +12V DC to the first injection amplifiers. U207 supplies +12V DC to the remaining +12V DC circuits. U208 supplies +6V DC to the remaining circuits.

6.1.3 HELICAL FILTER (L201-L203), RF AMPLIFIER (Q201)

The receive signal enters the receiver on coaxial connector A201. A helical filter consisting of L201, L202 and L203 is a three-pole bandpass filter tuned to pass only a narrow band of frequencies (806-824 MHz) to the receiver. This filter also attenuates the image and other unwanted frequencies.

Impedance matching between the helical filter and RF amplifier Q201 is provided by C201, C202 and a section of microstrip. Q201 amplifies the receive signal to recover filter losses and increases receiver sensitivity. Biasing for Q201 is provided by R201/R202/R203/R204 and C204 provides RF bypass. A 1.8 dB attenuator follows amplifier Q201. Additional filtering of the receive signal is provided by 3-pole helical filter L204-L206. A section of microstrip on the collector of Q201 and C205/C207 match the impedance from Q201 to 3-pole helical filter L204-L206.

6.1.4 FIRST MIXER (U201), CRYSTAL FILTER (Z201/Z202)

First mixer U201 mixes the receive frequency with the first injection frequency to produce the 52.95 MHz first IF. Since low-side injection is used, the injection frequency is 52.95 MHz below the receive frequency. Matching between filter L204-L206 and the mixer is provided by L228, C208 and C372. The output of U201 is matched to Z201 at 52.95 MHz by L207, C209 and C267.

Z201 and Z202 form a two-section, four-pole filter with a center frequency of 52.95 MHz and a -3 dB bandwidth of 15 kHz. This filter attenuates adjacent channels and other signals close to the receive frequency. The filter sections are a matched pair and the dot on the case indicates which leads connect together. Matching with Q202 is provided by C210, L209 and C270.

6.1.5 IF AMPLIFIER (Q202), CRYSTAL FILTER (Z203/Z204)

Q202 amplifies the 52.95 MHz IF signal to recover filter and mixer losses and improve receiver sensitivity. Biasing for Q202 is provided by R208/R209/R211/R313 and C211/C212/C213 provide RF bypass. The output of Q202 is matched to crystal filter Z203 at 52.95 MHz by C214, C293 and L211.

Z203 and Z204 form a two-section, four-pole filter with a center frequency of 52.95 MHz and a -3 dB bandwidth of 15 kHz. This filter establishes the selectivity of the receiver by further filtering the 52.95 MHz IF. The filter sections are a matched pair and the dot on the case indicates which leads connect together. Matching with U202 is provided by C215, C216, C301, L225 and R322.

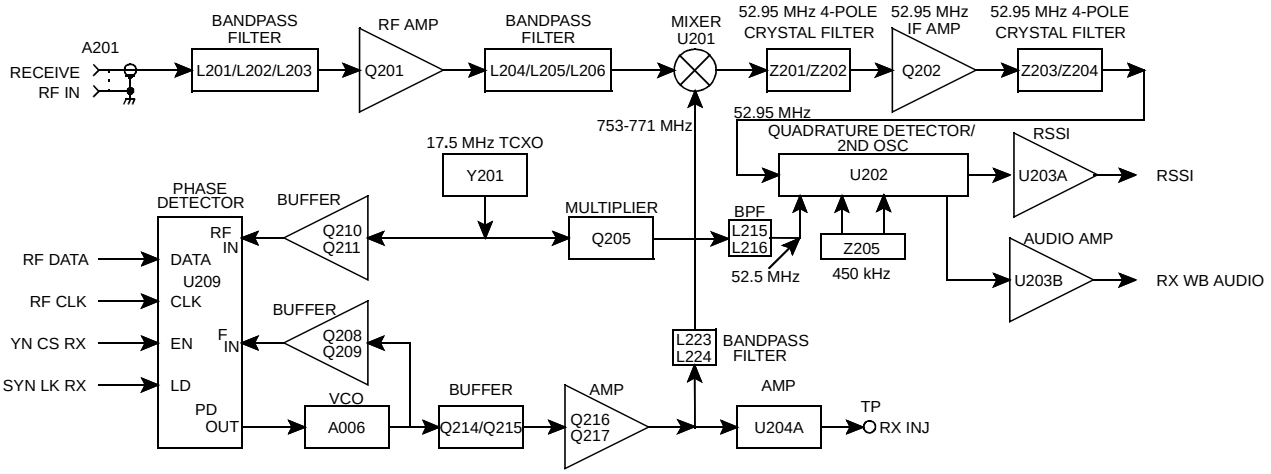


Figure 6-1 RECEIVER BLOCK DIAGRAM

6.1.6 SECOND MIXER/DETECTOR (U202)

As shown in Figure 6-2, U202 contains second oscillator, second mixer, limiter, detector and RSSI circuitry. The 52.95 MHz IF signal is mixed with a 52.5 MHz signal produced by TCXO Y201 and tripler Q205. The 17.5 MHz (±1 PPM) output of Y201 is fed through C231 to tripler Q205. The tripler passes the third harmonic at 52.5 MHz to the oscillator input of U202.

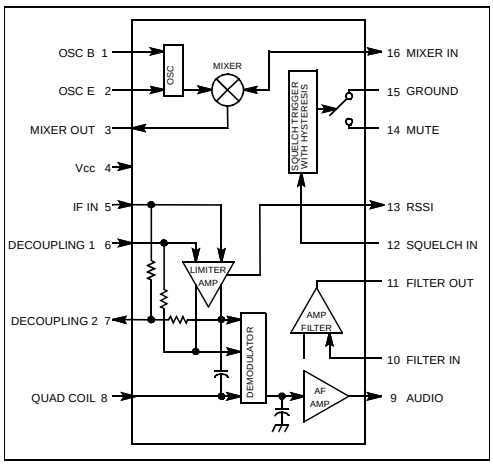


Figure 6-2 U202 BLOCK DIAGRAM

Biasing of Q205 is provided by R228, R227 and R229. RF choke L214 blocks the flow of RF through R229. An AC voltage divider formed by C236/C235 matches Q205 to the highpass filter. The third harmonic of the TCXO frequency is then used to drive the OSC B input at 52.5 MHz. L215, C237 and L216 for a high pass filter to attenuate frequencies below 52.95 MHz. C222 and C238 match the output of the filter to U202.

The 450 kHz second IF is then fed to ceramic filter Z205, then into the IF amplifier. The center frequency of Z205 is 450 kHz with a bandwidth of 15 kHz used to attenuate wideband noise. The limiter amplifies the 450 kHz signal 92 dB which removes any amplitude fluctuations.

From the limiter the signal is fed to the quadrature detector. An external phase-shift network connected to U202, pin 8, shifts the phase of one of the detector inputs 90° at 450 kHz (the other inputs are unshifted in phase). When modulation occurs, the frequency of the IF signal changes at an audio rate as does the phase of the shifted signal. The detector, which has no output with a 90° phase shift, converts the phase shift into an audio signal. Z213 is adjusted to provide maximum undistorted output from the detector. The audio signal is then fed out on U202, pin 9.

6.1.7 WIDEBAND AUDIO AMPLIFIER (U203B)

U203B amplifies the detected audio and data signal. R280/R263 set the gain of the amplifier and R256/R262/R284 provide a DC reference level. C220 bypasses the 450 kHz IF signal and C240 bypasses other frequencies. The output signal is adjusted by R264 and fed to J201, pin 9.

6.1.8 RSSI AMPLIFIER (U203A)

U202, pin 13 is an output from an internal RSSI (receive signal strength indicator) circuit which provides a current proportional to the strength of the 450 kHz IF signal. The RSSI output is buffered through U203A and the level is adjusted by R261. The DC output signal is then fed to J201, pin 7.

6.1.9 VCO (A006)

The Voltage-Controlled Oscillator (VCO) is formed by Q802 circuitry and a resonator consisting of L220 in the Receiver. The adjusting screw in L220 tunes the tank circuit to the desired frequency range. The VCO oscillates in a frequency range from 753-771 MHz. Biasing of Q802 is provided by R805, R806 and R807. AC voltage divider C812 and C813 initiates and maintains oscillation. C803 couples Q802 to L220 that provides the shunt inductance of the tank circuit. The shunt capacitance of the tank circuit is made primarily by C804 in series with CR802.

The VCO frequency is controlled in part by DC voltage across varactor diode CR802. As voltage across a reverse-biased varactor diode increases, its capacitance decreases. Therefore, VCO frequency increases as the control voltage increases. The control line is RF isolated from tank circuit by choke L804. The amount of frequency change produced by CR802 is controlled by series capacitor C804.

6.1.10 ACTIVE FILTER (Q801)

Q801 functions as a capacitance multiplier to provide filtering of the 12V supply to Q802. R801 and R802 provide transistor bias, and C809 provides the capacitance that is effectively multiplied by the gain of Q801. If a noise pulse or other voltage change appears on the collector, the base voltage does not change because of C809. Therefore, the base current does not change and transistor current remains constant. R803 decouples the VCO output from AC ground. L803 is an RF choke and C807, C808, C810 and C811 provide RF bypass.

6.1.11 BUFFER (Q208, Q209)

A cascode amplifier formed by Q208/Q209 provides amplification and isolation between the VCO and Synthesizer. A cascode amplifier is used because it provides high gain, high isolation and consumes only a small amount of power. The input signal to this amplifier is coupled from the VCO RF output on pin 4. DC blocking and coupling to the VCO is provided by C268 and to the buffer by C261. Bias for the amplifier is provided by R275, R279, R278 and R277. Q209 is a common-emitter amplifier and Q208 is a common-base with C260 providing RF bypass. L219 provides some filtering of the cascode output. R273 lowers the Q of L219. The output of the amplifier is coupled by C309 to U209, pin 11.

6.1.12 SYNTHESIZER (U209)

The synthesizer inputs/outputs are shown in Figure 6-3. The synthesizer output signal is the receiver first injection frequency. This signal is produced by a VCO (voltage-controller oscillator). The frequency of this oscillator is controlled by a DC voltage. This DC voltage is generated by integrating the pulses from the phase detector in synthesizer chip U209. This integration is performed by the synthesizer loop filter which is made up of C805, C806 and R804 in the VCO circuitry.

Frequencies are selected by programming counters in U209 to divide by a certain number. This programming is provided through J201, pins 12, 18 and 20. The frequency stability of the synthesizer is established by the ±1.0 PPM stability of TCXO Y201. The output of this oscillator is stable from 30°C to +60°C (-22°F to +140°F).

The VCO frequency of A006 is controlled by a DC voltage produced by integrating the phase detector output pulses of U209 The phase detector senses the phase and frequency of the two input signals (f_V and f_R) and causes the VCO control voltage to increase or decrease if they are not the same. When the frequencies are the same the VCO is "locked" on frequency.

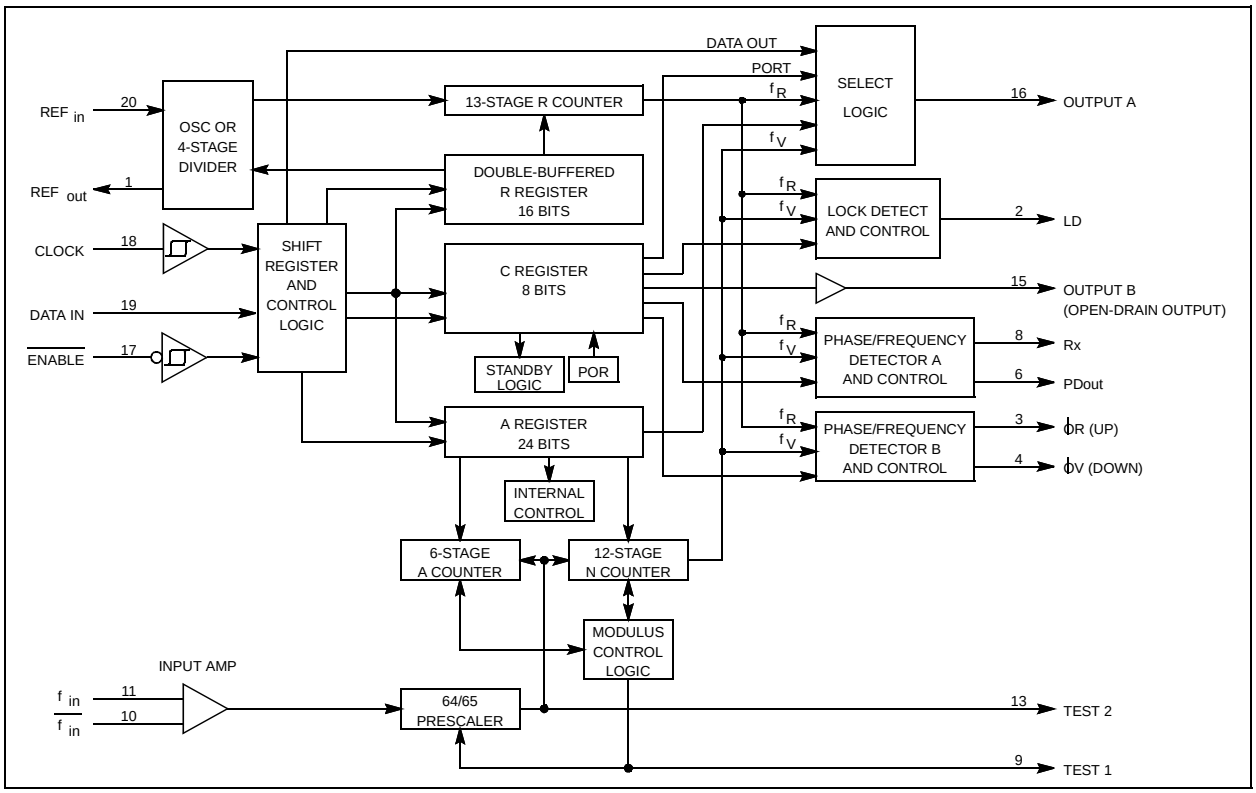


Figure 6-3 SYNTHESIZER BLOCK DIAGRAM

One input signal to the phase detector in U209 is the reference frequency (f_R). This is the 17.5 MHz TCXO frequency divided by the R (reference) counter to the channel spacing or 12.5 kHz.

The other input to the phase detector in U209 is from the VCO frequency divided down by the "N" counter and prescaler in synthesizer U209 to 12.5 kHz. The "N" counter is programmed through the synthesizer data line on J201, pin 20. U209 is programmed so that the phase detector input (f_V) is identical to the reference frequency (f_R) (12.5 kHz) when the VCO is locked on the correct frequency.

The synthesizer contains the R (reference), N, and A counters, phase and lock detectors and counter programming circuitry. Frequencies are selected by programming the three counters in U209 to divide by assigned numbers. The programming of these counters is performed by circuitry in the Main Processor Card (MPC), which is buffered and latched through the Interface Alarm Card (IAC) and fed into the synthesizer on J201, pin 20 to Data input port U209, pin 19.

Data is loaded into U209 serially on the Data input port U209, pin 19. Data is clocked into the shift registers a bit at a time by a low to high transition on the Clock input port U209, pin 18. The Clock pulses come from the MPC via the IAC to J201, pin 18.

As previously stated, the counter divide numbers are chosen so that when the VCO is operating on the correct frequency, the VCO-derived input to the phase detector (f_V) is the same frequency as the TCXO-derived input (f_R) which is 12.5 kHz.

The f_R input is produced by dividing the 17.5 MHz TCXO frequency by 1400. This division is done by the "R" counter in U209. The counter always divides by 1400 regardless of the channel number. This produces a reference frequency (f_R) of 12.5 kHz.

Since the VCO is on frequency (receive frequency minus 52.95 MHz) and no multiplication is used, the channel frequencies change in 12.5 kHz steps and the reference frequency (f_R) is 12.5 kHz for all channels selected by this receiver.

The f_V input is produced by dividing the VCO frequency using the prescaler and N counter in U209. The prescaler divides by 64 or 65. The divide number of the prescaler is controlled by the N and A counters in U209.

The N and A counters function as follows: both the N and A counters begin counting down from their programmed number. When the A counter reaches zero, it halts until the N counter reaches zero. Both counters then reset and the cycle repeats. The A counter is always programmed with a smaller number than the N counter. While the A counter is counting down, the prescaler divides by 65. Then when the A counter is halted, the prescaler divides by 64.

Example: Assume a receive frequency of 813.4875 MHz (channel 300). Since the VCO is 52.95 MHz below the receive frequency it must be 760.5375 MHz for channel 300. To produce this frequency, the N and A counters are programmed as follows:

N = 950 A = 43

NOTE: Section 8.2.5 describes how the N and A counter numbers can be calculated for other channels.

To determine the overall divide number of the prescaler and N counter, the number of VCO output pulses required to produce one N counter output pulse can be counted. In this example, the prescaler divides by 65 for 65 x 43 or 2,795 input pulses. It then divides by 64 for 64 x (950 - 43) or 58,048 input pulses. The overall divide number K is therefore (58,048 + 2,795) or 60,843. The VCO frequency of 760.5375 MHz divided by 60,843 equals 12.5 kHz which is the f_R input to the phase detector. The overall divide number K can also be determined by the following formula:
K = 64N + A

Where,
N = N counter divide number and
A = A counter divide number.

6.1.13 BUFFER AMPLIFIER (Q210, Q211)

A cascode amplifier formed by Q210 and Q211 provides amplification and also isolation between the TCXO and Synthesizer U209. A cascode amplifier is used because it provides high reverse isolation. The input signal to this amplifier is from TCXO Y201. C254 provides DC blocking. Bias for the amplifier is provided by R312, R248, R249, R251 and R250. L218 is an RF choke. RF bypass is provided by C251, C252 and C253. The output of Q210/Q211 is coupled to U209 by C307.

6.1.14 LOCK DETECT

When the synthesizer is locked on frequency, the Lock Detect output on U209, pin 2 is a logic high voltage with very narrow negative-going pulses. Then when the synthesizer is unlocked, these pulses become much wider, the width may vary at a rate determined by the frequency difference of f_V and f_R. The lock detect pulses are applied to J201, pin 14 and sent to the RF Interface on J103, pin 14 for detection and sampling in the IAC.

6.1.15 BUFFER AMPLIFIER (Q214, Q215)

A cascode amplifier formed by Q214 and Q215 provides amplification and also isolation between the VCO and Receiver RF stages. A cascode amplifier is used because it provides high reverse isolation. The input signal to this amplifier is coupled from VCO A006 by C268. C268 also provides DC blocking. Bias for the amplifier is provided by R294, R311, R290, R291 and R292. L222 is an RF choke and R293 lowers the Q of the coil. RF bypass is provided by C274, C356, C310, C272, C273 and C335. The output of Q214/Q215 is matched to the Receiver RF stages by C275, C276 and two sections of microstrip.

6.1.16 RF AMPLIFIERS (Q216, Q217)

U210 provides the +12V source for these amplifiers. RF amplifier Q216 is biased by R296 and R295. C278 provides RF bypass from the DC line and R297 provides supply voltage isolation. A section of microstrip on the collector acts as an RF inductor. Q216 is matched to Q217 by C277, C263, C288 and two sections of microstrip.

RF amplifier/buffer Q217 is similar in design to Q216. The output of Q217 is matched to the 3 dB attenuator made up of R285/R286/R287 by two sections of microstrip and C280 provides DC blocking. L223/L224 are tuned to the receive frequency -52.95 MHz and passed to Mixer U201. This injection frequency is also coupled through C284 to U204A. CR201, R255, R254 provide DC input to U204A, pin 3. The output of U204A, pin 1 is connected to J201, pin 13 for a receive injection test point and connected to the RF Interface Board on J103, pin 13.

6.2 EXCITER

6.2.1 VCO (A007)

The Voltage-Controlled Oscillator (VCO) is formed by Q802, associated circuitry and a resonator consisting of L404 in the Exciter. The screw in L404 in the Exciter tunes the tank circuit to the desired frequency range. The VCO oscillates in a frequency range from 851-869 MHz. Biasing of Q802 is provided by R805, R806 and R807. An AC voltage divider formed by C812 and C813 initiates and maintains oscillation. C803 couples Q802 to resonator L404 in the Exciter. Resonator L404 provides the shunt inductance of the tank circuit. The shunt capacitance of the tank circuit is made primarily of C804 in series with CR802. RF choke L805 completes the DC bias path to ground.

The VCO frequency is controlled in part by DC voltage across varactor diode CR802. As voltage across a reverse-biased varactor diode increases, its capacitance decreases. Therefore, VCO frequency increases as the control voltage increases. The control line is RF isolated from tank circuit by choke L804. The amount of frequency change produced by CR802 is controlled by series capacitor C804.

The frequency is modulated in a similar manner. The transmit audio/data signal is applied across varactor diode CR801 to vary the VCO frequency at an audio rate. C802 in series with CR801 determine the amount of modulation produced by the audio signal.

6.2.2 VCO AND TCXO FREQUENCY MODULATION

Both the VCO and TCXO are modulated in order to achieve the required frequency response. If only the VCO was modulated, the phase detector in U403 would sense the frequency change and increase or decrease the VCO control voltage to counteract the change (at the lower audio frequencies inside the closed loop bandwidth of the synthesizer). If only the TCXO frequency was modulated, the VCO would not track the higher audio frequencies (those beyond the closed loop bandwidth of the synthesizer). However, by modulating both the VCO and TCXO a flat audio response is achieved. Potentiometers R425 and R446 balance the modulating signals.

There are two 3.5V sources on the Exciter board; one is a reference for the modulation amplifier to the VCO, the other is for the modulation amplifier to the TCXO.

The reference voltage on U402B, pin 5 is sent to buffer U407B, J401, pin 9 to RFIB connector J102, pin 9. The voltage leaves the RFIB on J101, pin 14 to J2, pin 27 on the backplane, to the bottom connectors via pin 7 and finally to the MAC on P100, pin 7.

With reference to the ground on the Exciter, the 3.5V reference stability is maintained by U126B/C/D on the MAC. The 3.5V DC passes through summing amplifier U129B and transmit modulation gate U118D to P100, pin 29 (Tx MOD). P100, pin 29 is connected to backplane connector J2, pin 8 and RFIB connector J101, pin 22 to J102, pin 13. The transmit modulation and 3.5V reference enter the Exciter on J401, pin 13 and is routed to U402B, pin 6. R425 sets the TCXO modulation level. The modulation signal along with the 3.5V DC is applied to U402A, pin 2.

6.2.3 ACTIVE FILTER

Q801 functions as a capacitance multiplier to provide filtering of the 12V supply to Q802. R801 and R802 provide transistor bias, and C809 provides capacitance that is effectively multiplied by the gain of Q801. If a noise pulse or other quick voltage change appears on the collector, base voltage does not change significantly because of C809. Therefore, the base current does not change and transistor current remains

constant. R803 decouples the VCO output from AC ground. L803 is an RF choke and C807, C808, C810 and C811 provide RF bypass.

6.2.4 BUFFER (Q406, Q407)

A cascode amplifier formed by Q406/Q407 provides amplification and also isolation between the VCO and synthesizer. A cascode amplifier is used because it provides high reverse isolation. The input signal to this amplifier is tapped from the VCO RF output. DC blocking to the VCO is provided by C441 and to the buffer by C433. Bias for the amplifier is provided by R451, R453, R454 and R455. Q407 is a common-emitter amplifier and Q406 is a common-base with C432 providing RF bypass. L403 decouples the output from AC ground and R452 lowers the Q of L403. The amplifier is coupled by C429 and C499 to U403, pin 11.

6.2.5 SYNTHESIZER (U403)

The synthesizer inputs/outputs are shown in Figure 6-3. The synthesizer output signal is the transmit frequency. This signal is produced by a VCO (voltage-controller oscillator) that is frequency controlled by a DC voltage produced by synthesizer chip U403. This DC voltage is filtered by a loop filter made up of C805, C806 and R804 in the VCO circuitry.

Frequencies are selected by programming counters in U403 to divide by a certain number. This programming is provided through J401, pins 12, 19 and 20. The frequency stability of the synthesizer is established by the ±1.0 PPM stability of TCXO Y401. This oscillator is stable from -30°C to +60°C (-22°F to +140°F).

The VCO frequency of A007 is controlled by a DC voltage produced by the phase detector in U403. The phase detector senses the phase and frequency of the two input signals and causes the VCO control voltage to increase or decrease if they are not the same. When the frequencies are the same, the VCO is then "locked" on frequency.

The synthesizer contains the R (reference), N, and A counters, phase and lock detectors and counter programming circuitry.

One input signal to the phase detector in U403 is the reference frequency (f_R). This frequency is the 17.5 MHz TCXO frequency divided by the reference counter to the channel spacing or 12.5 kHz. The other input signal (f_V) is the VCO frequency divided by the "N" counter in U403. The counters are programmed through the synthesizer data line on J401, pin 20. Each channel is programmed by a divide number so that the phase detector input is identical to the reference frequency (f_R) when the VCO is locked on the correct frequency.

Frequencies are selected by programming the three counters in U403 to divide by assigned numbers. The programming of these counters is performed by circuitry in the Main Processor Card (MPC), buffered and latched through the Interface Alarm Card (IAC) and fed into the synthesizer on J401, pin 20 to Data input port U403, pin 19.

Data is loaded into U403 serially on the Data input port U403, pin 19 when U403, pin 17 is low. Data is clocked into the shift registers a bit at a time by a low to high transition on the Clock input port U403, pin 18. The Clock pulses come from the MPC via the IAC to J401, pin 19.

As previously stated, the counter divide numbers are chosen so that when the VCO is operating on the correct frequency, the VCO-derived input to the phase detector (f_V) is the same frequency as the TCXO-derived input (f_R). The f_R input is produced by dividing the 17.5 MHz TCXO frequency by 1187. This produces a reference frequency (f_R) of 12.5 kHz. Since the VCO is on frequency and no multiplication is used, the frequencies are changed in 12.5 kHz steps. The reference frequency is 12.5 kHz for all frequencies selected by this Exciter.

The f_V input is produced by dividing the VCO frequency using the prescaler and N counter in U403. The prescaler divides by 64 or 65. The divide number of the prescaler is controlled by the N and A counters in U403. The N and A counters function as follows:

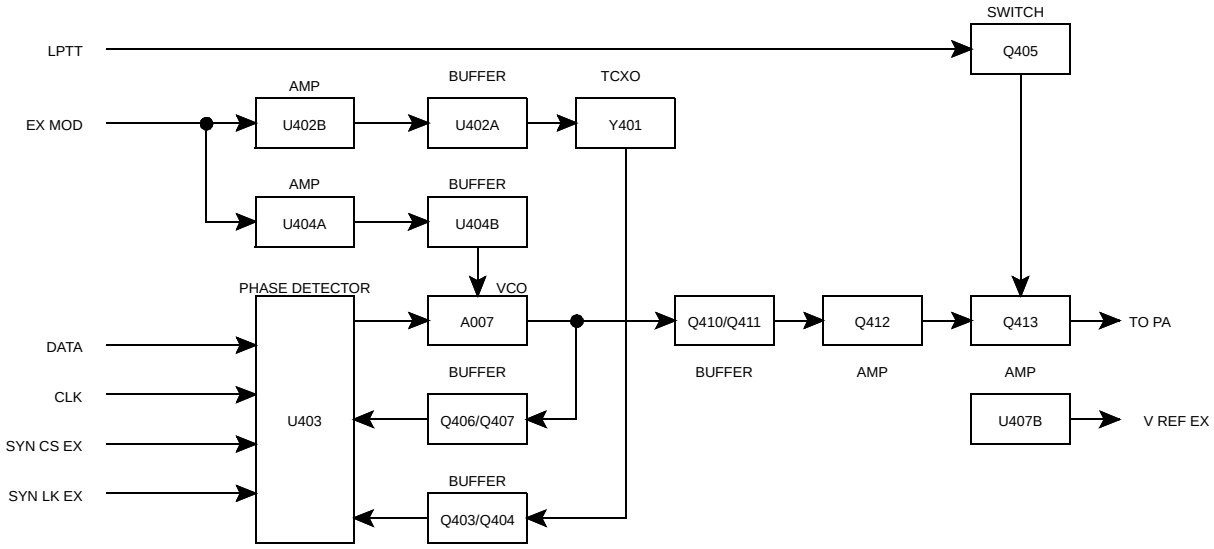


Figure 6-4 EXCITER BLOCK DIAGRAM

Both the N and A counters begin counting down from their programmed number. When the A counter reaches zero, it halts until the N counter reaches zero. Both counters then reset and the cycle repeats. The A counter is always programmed with a smaller number than the N counter. While the A counter is counting down, the prescaler divides by 65. Then when the A counter is halted, the prescaler divides by 64.

Example: To illustrate the operation of these counters, assume a transmit frequency of 858.4875 MHz (channel 300). Since the VCO is the channel frequency for transmit this frequency is used. To produce this frequency, the N and A counters are programmed as follows:

N = 1073 A = 7

To determine the overall divide number of the prescaler and N counter, the number of VCO output pulses required to produce one N counter output pulse can be counted. In this example, the prescaler divides by 65 for 65 x 7 or 455 input pulses. It then divides by 64 for 64 x (1073 - 7) or 68,224 input pulses. The overall divide number K is therefore (68,224 + 455) or 68,679. The VCO frequency of 858.4875 MHz divided by 68,679 equals 12.5 kHz which is the f_R input to the phase detector. The overall divide number K can also be determined by the following formula:
K = 64N + A

Where,
N = N counter divide number and
A = A counter divide number.

NOTE: Section 8.2.5 describes how the N and A counter numbers can be calculated for other channels.

6.2.6 BUFFER AMPLIFIER (Q403, Q404)

A cascode amplifier formed by Q403 and Q404 provides amplification and also isolation between the TCXO and Synthesizer U403. A cascode amplifier is used because it provides high gain, high reverse isolation and consumes only a small amount of power. The input signal to this amplifier is coupled from TCXO Y401, pin 5 by C420. C420 also provides DC blocking. Bias for the amplifier is provided by R430, R431, R432, R433 and R428. L402 is an RF choke. RF bypass is provided by C416, C418 and C419. The output of Q403/Q404 is coupled to U403, pin 20 by C417.

6.2.7 BUFFER AMPLIFIER (Q406, Q407)

A cascode amplifier formed by Q406 and Q407 provides amplification and also isolation between the VCO and Synthesizer U403. A cascode amplifier is used because it provides high gain, high isolation and consumes only a small amount of power. The input signal to this amplifier is coupled from VCO A007, pin 6 by C433. C433 also provides DC blocking. Bias for the amplifier is provided by R450, R451, R453, R454 and R455. L403 is an RF choke. RF bypass is provided by C430, C431 and C479. The output of Q406/Q407 is coupled to U403, pin 11 by a non-polarized capacitor formed by C429/C499.

6.2.8 LOCK DETECT

When the synthesizer is locked on frequency, the Lock Detect output on U403, pin 2 is a high voltage with narrow negative-going pulses. When the synthesizer is unlocked, the negative-going pulses are much wider, the width may vary at a rate determined by the frequency difference of f_V/f_R.

The locked or unlocked condition of the synthesizer is filtered by R440/C423 and applied to J401, pin 16, then sent to the RF Interface on J102, pin 16 for detection.

6.2.9 BUFFER AMPLIFIER (Q410, Q411)

A cascode amplifier formed by Q410/Q411 provides amplification and also isolation between the VCO and exciter RF stages. A cascode amplifier is used because it provides high gain, high isolation and consumes only a small amount of power. The input signal to this amplifier is tapped from VCO A007, pin 4 by C441. C441 also provides DC blocking. Bias for the amplifier is provided by R464, R465, R466, R467 and R468. L406 is an RF choke and R483 lowers the Q of the coil. RF bypass is provided by C434, C442, C445, C443, C444 and C480. The output of Q410/ Q411 is matched to the Exciter RF stages by C446, R450 and two sections of microstrip.

6.2.10 RF AMPLIFIERS (Q412, Q413)

RF amplifier Q412 is biased by CR402, R469, R470 and R472. C448 provides RF bypass from the DC line and R471/R472 provide supply voltage isolation. A section of microstrip on the collector acts as an RF choke to the supply line. Q412 is matched to Q413 by C449, C451 and two sections of microstrip.

RF amplifier/buffer Q413 is similar in design to Q412. The collector voltage of Q413 is switched by Q405. When the Logic Push-To-Talk (LPTT) on J401, pin 11 is low Q405 turns on and conducts the 15V supply to the collector of Q405 and to Q413. The output of Q413 is matched to 50 ohms by two sections of microstrip and C465 provides DC blocking. A 3 dB attenuator follows amplifier Q413. The RF output of the Exciter is on coaxial connector J402 to the Power Amplifier.

6.3 75W POWER AMPLIFIER

6.3.1 AMPLIFIER/PREDRIVER (U501)

RF input to the PA from the Exciter is through a coaxial cable and connector to WO511. C501 couples the RF to 50 ohm microstrip that connects the input to U501. U501 is a 6W amplifier/pre- driver operating in the 851-869 MHz range.

Power control is connected to WO505 from the RF Interface board (RFIB). RF is filtered from the control voltage line by various capacitors and inductors to U501, pin 2. This control voltage regulates the RF output of the amplifier on U501, pin 4 to approximately 5W.

6.3.2 DRIVER (Q501)

The output of U501 passes through several sections of 50 ohm microstrip and matching capacitors to the emitter of Q501. Driver Q501 is a common base amplifier with a normal output of approximately 22W. Supply voltage is RF bypassed by various capacitors and microstrip. C519, C520, C521 and microstrip match the output of the driver to 50 ohms at J501. A501 couples driver output to the input splitter of the finals.

6.3.3 FINAL AMPLIFIERS (Q502, Q503)

Q502 and Q503 are combined 60W amplifiers. The 22W RF input from J501 on the output of driver Q501 is applied to WO514 through a coaxial cable and connector. A 50 ohm microstrip connects the RF to a

70.7 ohm Wilkinson splitter and then to the emitter of each common-base amplifier. The 60W outputs on the collectors of the amplifiers are combined using a Wilkinson combiner. Q502 has a half-wave transmission line on the input and Q503 has a half-wave on the output. These T-lines are used to drive the 60W amplifiers out of phase. The output of the combiner is fed from WO513 directly to the forward/reverse power detect board.

The Wilkinson splitter and combiner provide the capability to split the drive input and combine the final outputs while maintaining isolation between the two final amplifiers. The combiner consists of two quarter-wave transmission lines and a balancing resistor. During normal operation, a signal of relatively equal phase and amplitude is present on both ends of the balancing resistor. Therefore, no current flows and no power is dissipated in the balance resistor. If one final failed, the other final of a pair would continue to function.

6.3.4 POWER DETECTORS (U504A, U502B)

Electromagnetic coupling is used to sample the output of each final amplifier. The RF is then fed to a rectifier to create a voltage indicative of the power output. The outputs of U504A and U502B are monitored by the repeater software through the RF Interface Board. If a final amplifier fails, the software will reduce the output power to prevent overdriving the remaining final amplifier.

6.3.5 THERMAL SENSOR (U503)

Thermal protection is provided by temperature sensor U503. The operating range of the sensor is from -30° C to 100° C (-22° F to 212° F). CR505 is used to reference U503 above ground to allow the sensor to read below 0° C. Amplifier U502A sends the output of U503 through WO509 to the RF Interface Board. The RF Interface Board reduces the power amplifier to half power (via the MPC) if the temperature reading is too high and turns the fan on and off (not via the MPC). The fan is turned on at approximately 50°C and off again at 42°C.

6.3.6 FORWARD/REVERSE POWER DETECT, CIRCULATOR, LOW-PASS FILTER

The power amplifier output is directly coupled to the forward/reverse power detect board via a jumper. The output then enters the circulator and exits to the low-pass filter board and the antenna jack for a minimum power output of 75W at the default setting. If an antenna is not connected, the circulator connects the output power to R685.

Forward and reverse power are electromag- netically coupled from the input and reflected ports of the circulator. R663/R680 calibrate the forward and reverse sense levels. The sensed levels are coupled to the RF Interface Board and software.

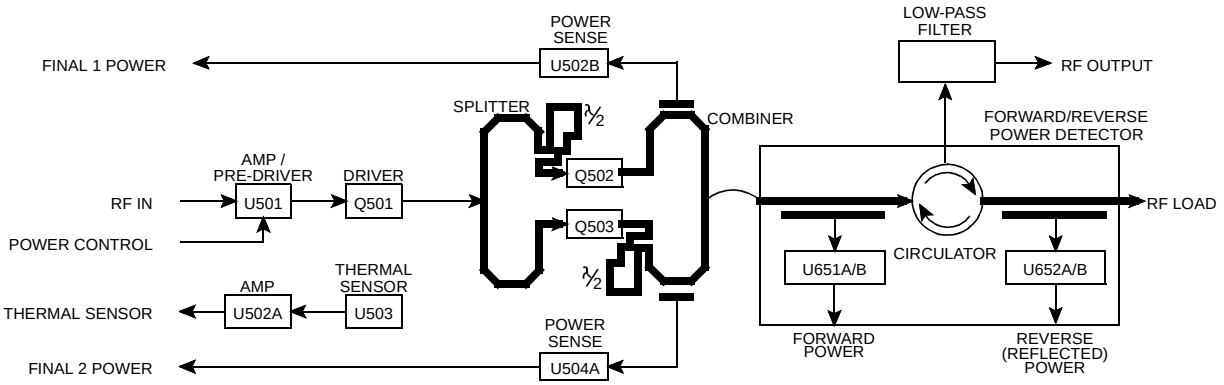


Figure 6-5 75W POWER AMPLIFIER BLOCK DIAGRAM

6.4 175W POWER AMPLIFIER

6.4.1 GAIN BLOCK (U501)

RF input to the PA from the Exciter is through a coaxial cable and connector to WO509. RF is directly coupled to 50 ohm microstrip that matches the input to U501. U501 is a 20W amplifier/pre- driver operating in the 851-869 MHz range.

Power control is connected to WO505 from the RF Interface board (RFIB). RF is filtered from the control voltage line by various capacitors and inductors to U501, pin 2. This control voltage regulates the RF output of the amplifier on U501, pin 5 to approximately 12W (see Figure 6-6).

6.4.2 DRIVER (Q502)

The output of U501 passes through several sections of 50 ohm microstrip and matching capacitors to the emitter of Q502. Driver Q502 is a common base amplifier with an output of approximately 60W. Supply voltage is RF bypassed by various capacitors and microstrip. C551 and C568 match the output of the driver to the input impedance of the splitter to the final amplifiers.

6.4.3 FINAL AMPLIFIERS (Q701, Q702, Q703, Q704)

The output of the driver is DC blocked through C552 and is connected to the first 70.7 ohm splitter with a 50 ohm microstrip. One output of the first splitter is sent directly to another 70.7 ohm splitter to feed Q703/Q704. The second output of the first splitter is connected to the splitter driving Q701/ Q702 through a half-wave 50 ohm microstrip. The 60W output of Q701/Q702 is combined through a 70.7 ohm quarter-wave Wilkinson combiner and fed through a 50 ohm microstrip to the final 50 ohm combiner.

Outputs from amplifiers Q703/Q704 are fed to the final combiner through 50 ohm microstrip that is a half-wavelength longer than the other side. The 25 ohm output impedance of the final combiner is transformed to 50 ohms through a quarter-wave, 35.35 ohm microstrip. The output of the quarter-wave transformer is fed directly into the forward power detector via W510.

The Wilkinson combiners provide the capability to split the drive input and combine the final outputs while maintaining isolation between the final amplifiers. Each combiner consists of two quarter-wave transmission lines and a balancing resistor. During normal operation, a signal of relatively equal phase and amplitude is present on both ends of the balancing resistor. Therefore, no current flows and no power is dissipated in the resistor. If one final failed, the other final of a pair would continue to function.

6.4.4 POWER DETECTORS

Electromagnetic coupling is used to detect the output of each final amplifier. The detected RF is then fed to a rectifier to create a voltage output indication of the power output. The outputs are monitored by the RF Interface Board and the station software. If any of the finals fails, the software will reduce the output power to prevent overdriving the remaining final amplifier.

6.4.5 THERMAL SENSOR (U503)

Thermal protection is provided by temperature sensor U503. The operating range of the sensor is from 0 to 100° C (32° F to 212° F). Amplifier U502A sends the output of U503 to WO519 and to the RF Interface Board. The RF Interface Board reduces the power amplifier to half power (via the MPC) if the temperature reading is too high and turns the fan on and off (not via the MPC). The fan is turned on at approximately 50°C and off again at 42°C.

6.4.6 FORWARD/REVERSE POWER DETECT, CIRCULATOR, LOW-PASS FILTER

The power amplifier output is directly coupled to the forward/reverse power detect board via a jumper. The output then enters the circulator and exits to the low-pass filter board and the antenna jack for a power output of 175W (±7W). If an antenna is not connected, the circulator connects the output power to R685.

Forward and reverse power is electromagnetically coupled to the detectors on the input and reflected ports of the circulator. R663 and R680 calibrate the forward and reverse sense levels. The sensed levels are coupled to the RF Interface Board and software.

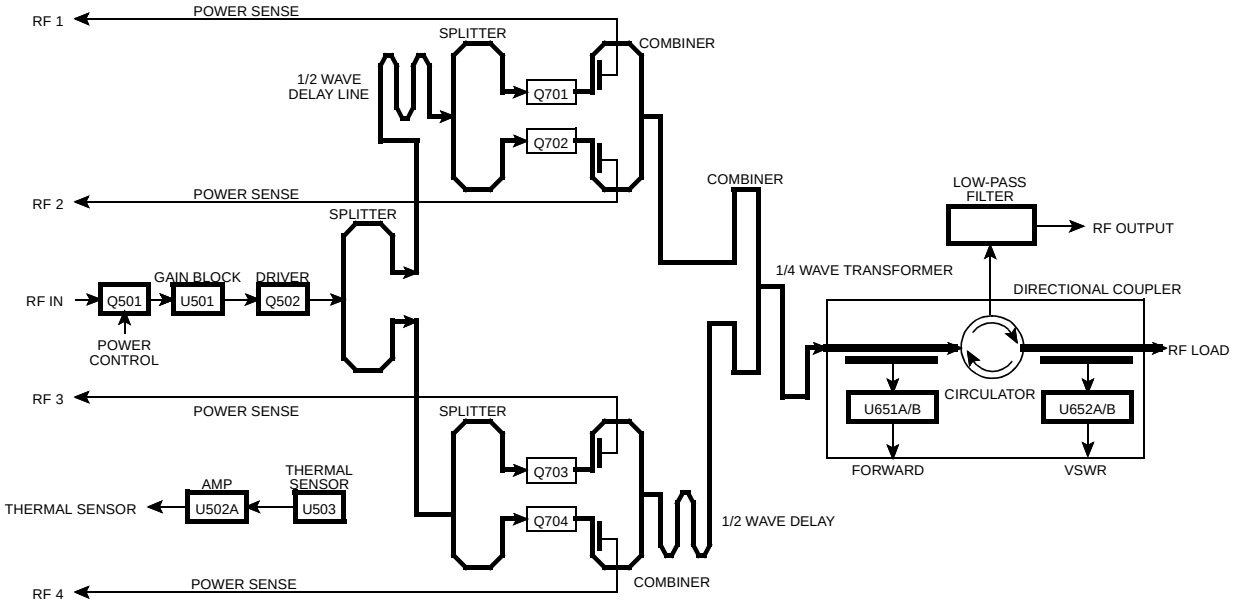


Figure 6-6 POWER AMPLIFIER BLOCK DIAGRAM

6.5 RF INTERFACE BOARD

The RF Interface Board (RFIB) connects the Receiver, Exciter and Power Amplifier to the back-plane and power supply (see Figure 6-7).

The input and output connectors for the RF Interface Board are defined as follows.

6.5.1 POWER CONNECTOR

The power supply is connected to the RF Interface Board when the RF module is inserted into the station cabinet (see Figure 10-5). The jack portion of the connection is on the RF Interface Board, the plug portion is attached to the station cabinet.

P101/P102 +26.5V DC - Supply voltage to PA. +26.5V ±1%, 12A at 75W and 25A at 175W.

P103 +15V DC - Supply voltage to Exciter, Receiver and Power Control. 15V ±1%, 5.5A max.

P104/P105 GROUND - Ground return for the RF assembly.

6.5.2 SIGNAL CONNECTOR (J101)

This is the signal interface connector (36 pin) that connects the RFIB to the backplane connector J2 (34 pin) through cable assembly A8.

Pin 1 GROUND

Pin 1 carries ground current between the RF Interface board and Backplane board.

Pin 2 PC STR

Pin 2 is the power Control Strobe. This is normally low until after the power control data is shifted into the power control register. Then the strobe line goes high and back to low. The clock or data lines cannot be changed until after the strobe is set.

Pin 3 HS CS EX

Pin 3 is not used at this time.

Pin 4 GROUND

Pin 4 carries ground current between the RF Interface board and Backplane board.

Pins 5-6 UNUSED

Pin 7 RX WBAND

The wide band audio is from the receive audio demodulator U202 and goes to the MAC in the Controller card cage. The typical amplitude is 387 mV RMS (-6 dBm) and 2V DC with Standard TIA Test Modulation into the receiver. Little wave shaping is done on the receiver board other than a 31 kHz RC LPF which strips off the 450 kHz IF. Buffering is done with an op-amp.

Pin 8 RF DATA A

Data A (U105, pin 11) is the least significant bit (LSB) in the 3 multiplex chips located on the RFIB. This pin is a CMOS input from the Controller requiring a logic high for activation.

Pin 9 RF DATA C

Data C (U105, pin 9) is the most significant bit (MSB) in the 3 multiplex chips located on the RFIB. This pin is a CMOS input from the Controller requiring a logic high for activation.

Pin 10 RF MUX2 INH

The Multiplexer-2 Inhibit (U106, pin 6) is a CMOS input from the Controller that inhibits (disables) the output from the RF 2 Multiplexer with a logic high.

Pin 11 RF CLK

The clock will control the synthesizer chip and power control circuit when loading. This pin is a TTL input from the Controller.

Pin 12 HS CS RX

Pin 12 is not used at this time

Pin 13 RF MUX1 INH

The Multiplexer-1 Inhibit (U105, pin 6) is a CMOS input from the Controller that inhibits (disables) the output from the RF 1 Multiplexer with a logic high.

Pin 14 V REF EX

This is the 3.5V reference to the Exciter TCXO. 3.5V from the Exciter is passed from J102, pin 9 to this pin and the backplane. The voltage then passes through the MAC and back to the backplane to J101, pin 22 with the TX MOD. These are connected to J102, pin 13 back to the Exciter.

Pins 15-18 UNUSED

Pin 19 RF MUX3 INH

The Multiplexer-3 Inhibit (U104, pin 6) is a CMOS input from the Controller that inhibits (disables) the output from the RF 3 Multiplexer with a logic high.

Pin 20 LPTT

The Logic Push-To-Talk is an open collector from the Controller. It has a sink capability of 20 mA and a maximum voltage rating of 18V. The transmitter should produce power when this pin is a logic low.

Pin 21 SYN CS EX

This input goes low to enable the loading of data into the exciter synthesizer chip U403.

Pin 22 TX MOD

The audio from the MAC in the Controller processes a number of inputs to the station to produce the signals on this pin. This signal goes through the RFIB and then to the Exciter. A 707 mV RMS sine wave (2V P-P) at 1 kHz produces 60% of system deviation in the transmitter. The source impedance is low and the input impedance is less than 10k ohms.

Pin 23 GROUND

Pin 23 carries ground current between the RFIB and Chassis Backplane.

Pin 24 UNUSED

Pin 25 LOGIC CONTROL TO FANS

Pin 25 is in parallel with the temperature sensor.

Pin 26 RF DATA B

The Data B (U105, pin 10) is the middle significant bit in the three multiplex chips located on the RFIB. This pin is a CMOS input from the Controller requiring a logic high for activation.

Pin 27 A D LEVEL

20 lines (of the possible 24) of RF functions sampled are multiplexed to the Controller through this pin using three multiplex chips.

- RF Forward Power Sense
- RF Power Sense Device 1
- RF Power Sense Device 2
- RF Power Sense Device 3
- RF Power Sense Device 4
- RF Reflected Power Sense
- PA Temperature
- Transmit Audio Modulation
- High Stability Exciter Lock Detector
- Exciter Lock Detector
- Receiver Detector Audio
- Receive Signal Strength Indicator
- Receiver Injection Level
- High Stability Receive Lock Detector
- Receiver Lock Detector
- Fan Current 1
- Fan Current 2
- Fan 1 On Sense
- Power Supply Temp
- Battery Voltage

Pin 28 RF DATA

A data pin with TTL levels from the Controller which has the dual role of loading the synthesizer chips and adjusting the power control D/A lines for proper output power. Up to four synthesizer chips and a shift-register could be connected to this pin.

Pin 29 SYN CS RX

This input goes low to enable the loading of data into the receiver synthesizer chip U209.

Pin 30 RSSI

This pin is the Receive Signal Strength Indication to the Controller. This RSSI is used for tune-up of the Receiver front-end during factory test mode. The dynamic range is 60 dB. It has an output from an op-amp with the voltage going from 0.5V to 4.5V. The level has an adjustment in the Receiver.

Pin 31 GROUND

Pin 31 carries ground current between the RFIB and Chassis Backplane.

Pins 32-36 UNUSED

6.5.3 FAN CONNECTOR (J104)

The outputs to the fan connectors are 4-pin plug-in terminals that supply DC voltage. The plug on the fan is a 2-pin connector. The plug-in terminals are located on the back of the RFIB.

Pin 1 FAN 1 LOW

Pin 1 is the ground return for Fan 1.

Pin 2 FAN HI

Pin 2 carries the voltage to Fan 1. The current is 1/4A nominal at 20V to 30V. This pin goes high when the PA heat sensor rises above 50°C and goes low below 45°C.

Pin 3 FAN2 LO

Pin 3 is the ground return for Fan 2 in 175W repeaters.

Pin 4 FAN HI

Pin 4 carries the voltage to Fan 2 in 175W repeaters. The Voltage is 20V-30V at 1/4A nominal. Pin 4 goes high when the PA heat sensor rises above 50°C and goes low below 45°C.

6.5.4 POWER AMPLIFIER CONNECTIONS

WO 115 POWER SENSE

This capacitive feedthrough pin is at +15V DC to the Power Detect Board.

WO 116 +26.5V DC

This capacitive feedthrough pin is at +26.5V DC and carries the PA current, 25A nominal at 175W from P102 to the Power Amplifier board.

WO 117 +26.5V DC GROUND

This capacitive feedthrough pin carries ground current from P105 to the Power Amplifier board. It must be capable of carrying up to 25A.

W118 +15V DC

This capacitive feedthrough pin connects +15V DC P103 to the PA, Exciter, and Forward/Reverse Power Detect boards. Maximum current handling is 6A (4A nominal at 175W).

WO 119 NOT USED

WO 120 CTRL OUT

This capacitive feedthrough pin carries the output of the power control driver on the RFIB to the power control pin of the power module on the Power Amplifier board. The voltage varies from 0V-15V with current as high as 0.5A.

WO 121 FWD PWR

This capacitive feedthrough pin is the forward power sense line. It is a voltage source that is a function of the output power of the Power Amplifier. The voltage level will be between 0V-5V and drive a 10k ohm load. A typical voltage of 3.9V correlates to 160W out of the PA. This line goes through the multiplexers and A D LEVEL line to the Controller for processing.

WO 122 RF OUT 1

This capacitive feedthrough pin is a voltage source that is a function of the output power of Q701. The voltage level will be between 0V-5V and drive a 10k ohm load. This line goes through the multiplexers and A D LEVEL line to the Controller for processing.

WO 123 RF OUT 2

This capacitive feedthrough pin is a voltage source that is a function of the output power of Q702. The voltage level will be between 0V-5V and drive a 10k ohm load. This line goes through the multiplexers and A D LEVEL line to the Controller for processing.

WO 124 RF OUT 3

This capacitive feedthrough pin is a voltage source that is a function of the output power of Q703. The voltage level will be between 0V-5V and drive a 10k ohm load. This line goes through the multiplexers and A D LEVEL line to the Controller for processing.

WO 125 RF OUT 4

This capacitive feedthrough pin is a voltage source that is a function of the output power of Q704. The voltage level will be between 0V-5V and drive a 10k ohm load. This line goes through the multiplexers and A D LEVEL line to the Controller for processing.

WO 126 REFL PWR

This capacitive feedthrough pin is the reflected power sense line. It is a voltage indicative of the power reflected due to a mismatch. The voltage produced will typically be such that less than a 3:1 VSWR will not trigger alarms and when VSWR = 6:1 the controller will reduce power. The voltage level will be between 0V-5V and drive a 10k ohm load. This line goes through the multiplexers and A D LEVEL line to the Controller for processing. The time to sense and reduce the power takes several seconds.

WO 127 TEMP

This capacitive feedthrough pin is the temperature sense line of the Power Amplifier. It will be a linearly variable function of temperature ranging from

0V-5V output and 0°C to +100°C (+32°F to 212°F) input when driving a 10k ohm load. The primary functions of this line are for fan on/off and PA power reduction. The fan should be turned on at 50°C and off at 45°C. The PA should have power reduced when 90°C (194°F) is reached and with absolute turn-off at 95°C (203°F). This line goes through the multiplexers and A D LEVEL line to the Controller for processing.

WO147 RF DETECT PRE-DRIVER

This senses power out of the pre-driver. It is used to limit the power out of the pre-driver to 0.6 dB over 175W at room temperature. The 75W repeater limits to 0.6 dB over 75W.

WO143 +26V DC

This is the +26.5V DC source to the RFIB from P101.

WO144 +15V DC

This is the +15V DC source to the RFIB from P103.

WO145 GROUND

W145 carries ground current from P104 to the RFIB.

6.5.5 EXCITER CONNECTOR (J102)

The connector from the Exciter (J401) to the RF Interface board (J102) links the Exciter to the MPC in the Controller Backplane.

Pin 1 VCC1

The voltage on this pin is a fused +15V ±1%, nominal current of 0.5A. It provides current to the Exciter from the RFIB.

Pins 2-8 GROUND

Pin 9 +3.5V DC

Pin 9 is the +3.5V DC TCXO reference voltage from the Exciter to the MAC.

Pin 10 GROUND

Pin 11 LPTT

The Logic Push-To-Talk (LPTT) is an open collector from the Controller. It has a sink capability of 20 mA nominal and a voltage rating of 18V maximum. The transmitter should produce power when this pin is a logic low.

Pin 12 SYN CS EX

Pin 12 is the Exciter synthesizer chip select. It allows data input to the synthesizer chip when the line is pulled to a logic low.

Pin 13 TX MOD

The audio from the MAC in the Controller processes a number of inputs to the station per the TIA specifications to produce the signal on this pin. This signal goes through the RFIB to the Exciter. A 707 mV RMS (2V P-P) sine wave at 1 kHz provides 60% of system deviation in the transmitter. The DC voltage on the line is 3.5V ±0.1V. The source impedance should be low (output of an op-amp or analog switch < 200 ohms) and the input impedance will not be less than 10k ohms.

Pins 14-15 GROUND

These pins carry ground current between the RFIB and the Exciter board.

Pin 16 SYN LK EX

Pin 16 is the Exciter synthesizer lock detector output. The synthesizer is locked with a TTL logic high state.

Pin 17 HS LK EX

Pin 17 is not used at this time.

Pin 18 HS CS EX

This input is not used at this time.

Pin 19 RF CLK

The clock controls the Exciter synthesizer when loading. The input source in the Controller is TTL with the speed determined by the synthesizer chip. There could be as many as four synthesizers and a shift register.

Pin 20 RF DATA

Pin 20 is a data pin from the Controller which has the dual role of loading the synthesizer chip and adjusting the power control D/A lines for proper output power. The data has TTL levels. Up to four synthesizer chips and a shift register could be connected to this pin.

6.5.6 RECEIVER CONNECTOR (J103)

The connector from the Receiver (J201) to the RF Interface board (J103) links the Receiver to the MPC in the Controller Backplane.

Pin 1 VCC1

Pin 1 is fused +15V ±1% with a nominal current of 1A provides current from the RFIB to the Receiver.

Pins 2-6 UNUSED

Pin 7 RSSI

This pin is the Receive Signal Strength Indicator (RSSI) to the Controller. The RSSI is used for tune-up of the Receiver front-end during test mode. The dynamic range is 60 dB. Output from an op-amp with the voltage going from 0.5V to 4.5V. The level has an adjustment in the Receiver.

Pin 8 UNUSED

Pin 9 RX WBAND

The receive wide band audio is from the demodulator and goes to the Main Audio Card (MAC) in the Controller card cage. The typical amplitude is 387 mV RMS (-6 dBm) and 2V DC with Standard TIA Test Modulation into the Receiver. Little wave shaping is done on the Receiver board other than a 31 kHz RC LPF which strips off the 450 kHz IF. Buffering is done with an op-amp which can drive a 10k ohm load.

Pin 10 UNUSED
Pin 11 GROUND

Pin 11 carries ground current between the RFIB and the Receiver board.

Pin 12 SYN CS RX

Pin 12 is the Receiver synthesizer chip select. This chip is the same part as used in the Exciter. A low enables loading the Synthesizer.

Pin 13 RX INJ

This pin is the power sense for the Receiver injection. It is a linear voltage source that is a function of the injection power. The voltage level will be between 0V - 5V and be able to drive a 10k ohm load.

Pin 14 SYN LK RX

Pin 14 is the main synthesizer lock detector output for the Receiver. The synthesizer is locked with a TTL logic high state.

Pin 15 GROUND

Pin 15 carries ground current between the RFIB and the Receiver board.

Pin 16 HS CS RX

Pin 16 is not used at this time.

Pin 17 GROUND

Pin 17 carries ground current between the RFIB and the Receiver board.

Pin 18 RF CLK

The clock controls the Receiver synthesizers when loading. The input source in the Controller is TTL with the speed determined by the synthesizer chip.

Pin 19 HS LK RX

Pin 19 is not used at this time.

Pin 20 RF DATA

Pin 20 is a data pin from the Controller which has the dual role of loading the synthesizer chips and adjusting the power control D/A lines for proper output power. The data has TTL levels. Up to four synthesizer chips and a shift register could be connected to this pin.

On the back of the card rack is the Backplane with plug-in connectors to the cards and cables to the RF modules, Power Supply and External Connector Board.

Refer to the component layout and schematic diagram in Section 10 for more information on the repeater backplane.

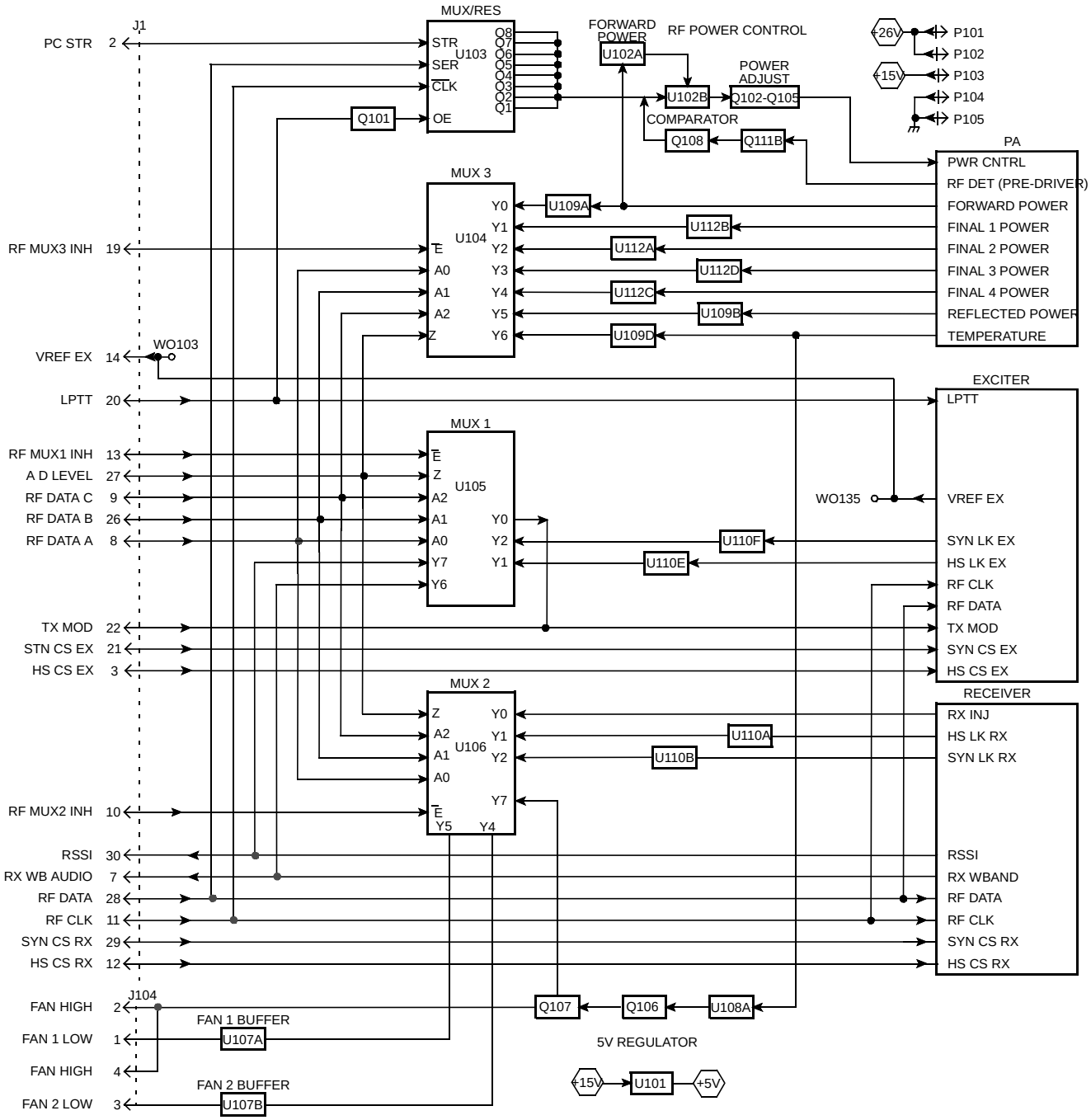


Figure 6-7 RF INTERFACE BOARD BLOCK DIAGRAM

6.6 800W POWER SUPPLY

WARNING

This power supply contains voltage potentials greater than 400V. Considering the dangerous voltages and the complexity of the switch-mode power supply, it is strongly recommended the power supply be returned to E.F. Johnson for repair (see Section 1.7).

6.6.1 FILTER BOARD

AC power is brought into the power supply through the IEC connector in the front of the power supply (see Figure 2-8). This connector is attached to the EMI filter assembly, Part No. 023-2000-820. The filter contains common mode and differential mode filtering such that the supply complies with FCC Class-A regulations. In addition to the filter components (C1, C2, L1, C3, C4, L2, C5) R1 is used to discharge the filter capacitors when AC is removed. Metal-oxide varistors (RV001/RV002) are placed across the line on the input and output of the EMI filter that clamp transients on the AC line to prevent damage to the power supply. The AC power is fused with F001 after the connector and before the filter. Replace fuse with a 15A/250V (314015) fuse.

At the output of the filter board is a bridge rectifier. The rectifier is heat sunk to the filter bracket through a Grafoil thermal interface pad. Filtered AC power is connected to the main board via wires W001 and W003. Filter and rectified current is brought to the main board via wires W004 and W005. The safety ground is connected from the filter board to a stud in the chassis through W002.

6.6.2 POWER FACTOR CORRECTION

The power factor switching frequency is set at 87.5 kHz, ±5 kHz. The average current mode boost converter is comprised of L107, Q101, CR145, C110, C111. Half of U102 is used for power factor correction. RT101/RT102 are negative temperature coefficient thermistors that limit the in-rush current to C110/C111. The resistor network connected to CR104 charges up C106/C107 to +18Voff the line. This provides the bias voltage required to start the controller IC U102. Once the IC turns on current is being switched on L107. A small tap winding on L107 provides sustaining current to the U102. When AC is first connected it could take several seconds for C106/C107 to charge to +14V before the unit starts.

U102 samples the input voltage through R105/R106/R107; the input current through T103/T104/CR146/CR108/R113/R114; and the output voltage through the divider at R127. U102 modulates the duty cycle to MOSFET Q101 such that the input current is shaped like and in phase with the input voltage. The controller has two feedback loops; a voltage loop to keep the 400V constant and a current loop to keep input current correct. Compensation for the current error amp is C120/R141/C121 on U102, pin 1. Compensation for the voltage error amp is provided by C127/C142/C126 on U102, pin 16. U102, pin 4 and associated circuitry automatically adjust the Power Factor Correction (PFC) for input voltage (100-240V AC), line frequency (50-60 Hz) and load on the power factor.

NOTE: The output voltage of the power factor section is at 400V DC. This voltage is bled off slowly. After turning off, it can take more than 5 minutes to discharge.

6.6.3 MAIN PULSE WIDTH MODULATOR

The +26.5V output is created from a two-transistor forward converter Q116/Q118. It uses the 400V output of the power factor correction on C110/C111 for an input voltage. The same controller IC (U102) drives the +26.5V stage. This stage runs at exactly twice the power factor correction frequency and uses trailing edge modulation. The pulse width modulator uses the PFC supplied current for modulation scheme that reduces ripple current in C110/C111.

The output of the IC, U102, pin 11 is fed to a level shifting gate drive network comprised of C139, C140, T106, C136, C197, C137 and C228. Each MOSFET (Q116, Q118) of the two-transistor forward converter has a gate protection zener diode CR117, CR120 respectively. In addition, each power MOSFET has a gate turnoff network.

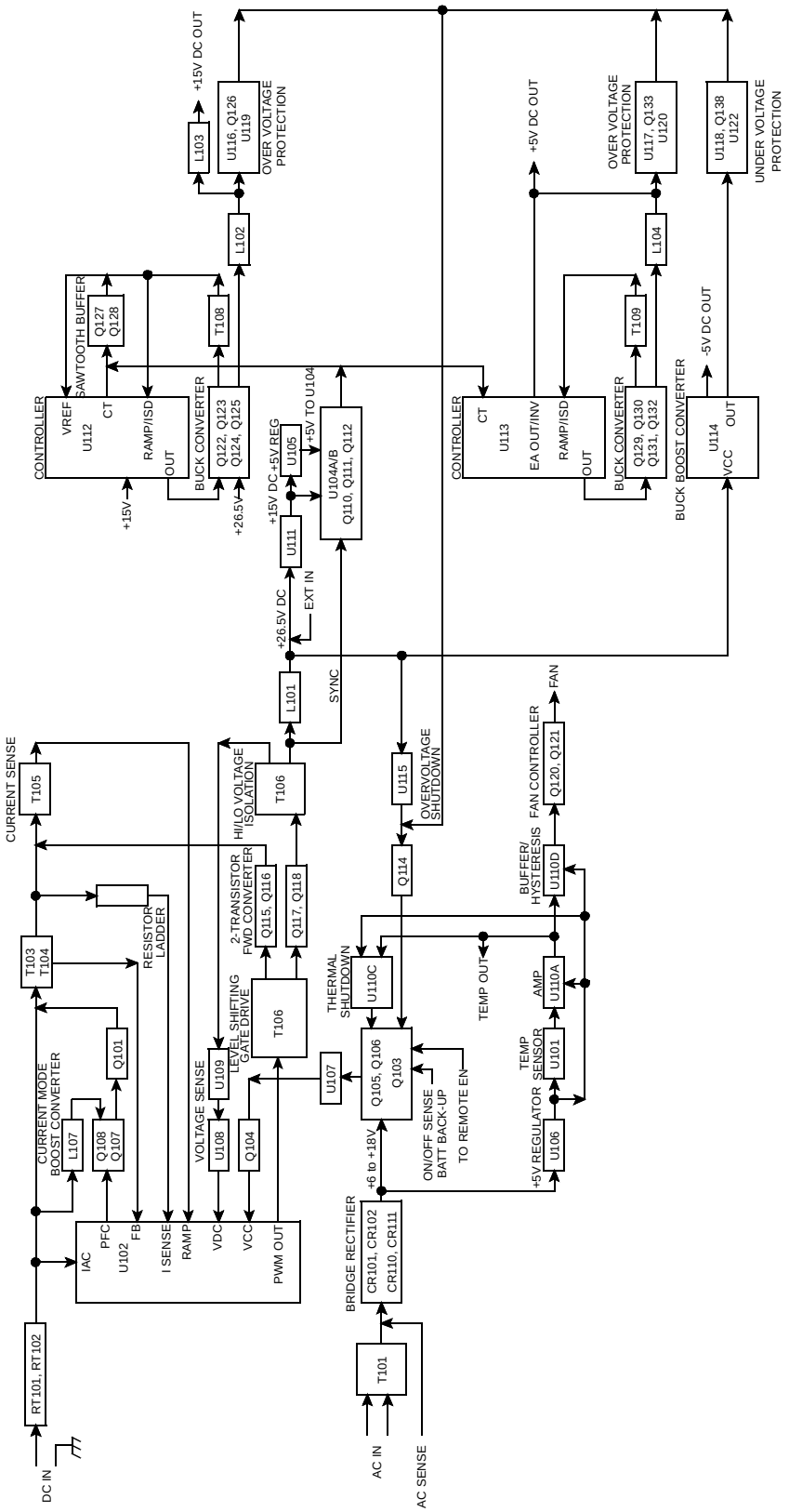


Figure 6-8 BLOCK DIAGRAM

In operation, the power MOSFETs Q116, Q118 are on for approximately one-third of the period providing current to the primary side of T107. During that time CR121 is forward conducting and charging L101. When the MOSFETs are switched off, the magnetizing current of T107 continues to flow through CR118, CR119. These diodes place 400V across the transformer in opposite polarity that resets the transformer core. During the off period CR128 is free wheeling and L101 is discharging. Transformer T107 provides the isolation between the low voltage and high voltage sections.

The +26.5V pulse width modulator is peak current mode controlled. This type of converter requires current and voltage sense. T105, CR112, R125, R146 and C125 provide the current sense circuit. The voltage sense circuit is U109 and the associated circuitry on the isolated side of the supply.

An opto-isolator is used to cross the boundary from high to low voltage sections. In the event of an over-voltage condition (>+32V) U115 and associated components turn the power supply off. This shutdown mechanism latches the power supply Off. The enable line must be turned Off for 10 seconds for the power supply to reset. T106 has a tap to provide current to the optional battery back-up (Part No. 023-3-2000-830). The +26.5V is available at the high current output connector to the power supply and it also powers the +15V, +5V and -5V converters through F102.

6.6.4 SYNCHRONIZING CIRCUITS

The +15V and +5V sections run at the same frequency as the +26.5V pulse width modulator. In order for a beat note not to be produced, a sync circuit is used. If two converters are not synchronized, the difference frequency may show up at an undesired location in the repeater.

Divider R151/R152 samples the output of the main pulse width modulator. When Q116 and Q118 turn on, the output on U104A, pin 3 goes high. C138, R176, CR122 along with U104B creates a very narrow pulse on U104B, pin 6. Q110, Q111 and Q112 level shift and buffer this pulse. When the narrow pulse is presented to the timing capacitor of the +15V and +5V converters, the cycle terminates and a new one starts. This forces the +15V and +5V converters to run at the same frequency and is slightly delayed from the +26.5V converter.

6.6.5 FAN AND THERMAL SHUTDOWN

The voltage supply to the thermal measurement circuit is generated from transformer T101 and the associated bridge rectifier consisting of CR101, CR102, CR110 and CR111 and bulk storage capacitor C101. This voltage is approximately +9V when the AC voltage is at 120V AC.

NOTE: This DC voltage is dependant on the input AC voltage.

U106 provides a very accurate +5V required for proper operation of the temperature sense circuit. A precision temperature sensor (U101) is mounted to the +26.5V rectifier heatsink. The output of this sensor is 10 mV/°C with a ±1% accuracy. This voltage is amplified by U110A with precision resistors R183/R184 setting the gain.

The output of gain stage U110A is fed to the computer interface via WO116 to monitor power supply temperature with the programmer. The output of U110A, pin 3 is also connected to the thermal shutdown circuit U110C, R135, R136, R137, R138 and R139. If the heatsink temperature reaches 92°C (198°F) the output of U110C, pin 8 goes high and saturates Q103. When Q103 is turned on U107 is turned off and the power supply turns off. The remote voltage is always present so when the heatsink temperature drops to 80°C (176°F) the power supply restarts. The high temperature condition would only exist if the fan was blocked or faulty.

The output of U110A, pin 1 also connects to the fan controller. U110D with the associated resistors provides a means to turn the fan on/off. Transistors Q120/Q121 provide current gain and a voltage level shift to run the fan. The fan turns on when the heatsink reaches approximately 45°C (113°F) and turns off again when the temperature reaches 35°C (95°C). In normal operation the fan turns on and off.

6.6.6 +15V CONVERTER

The input voltage to this "Buck" DC/DC converter is the main +26.5V output fused through F102. The bias voltage for the controller IC U112, pin 15 is provided by a +15V regulator U111. The basic buck converter consists of MOSFET Q125, Schottky diode CR126 and storage inductor L102. C165, C166, C167, L103, C169 and C170 filter the output voltage and attenuate the ripple at the switching frequency (160 kHz). The capacitors are an integral part of the feedback loop. The duty cycle is approximately 60%.

The +15V buck converter is peak current mode controlled. T108 samples the inductor current while MOSFET Q125 is on. The sampled current is translated to a voltage via CR127, R209 and R210.

Because the MOSFET is a high-side switch, a charge pump is required to get the gate voltage above the input voltage. The charge pump operates as follows. When the output from IC U112, pin 14 is low, capacitor C162 is charged through CR124, R198, R199, R200 and Q122/Q123 are off. When U112, pin 14 goes high, the capacitor stays charged and CR124 is reverse biased. Q122/Q123 are turned on forward biasing CR125 and applying a gate-to-source voltage of approximately +12V. During this time Q124 is off. When U112, pin 14 goes low, Q124 turns on and rapidly discharges the gate capacitance.

Resistors R231/R208 coupled with C164 provide snubbing for Schottky diode CR126.

Because the +15V converter operates at greater than 50% duty cycle, slope compensation is required. Capacitor C176 is the time capacitor for this converter and R223 is the resistor that sets the charge current. A sawtooth wave is present on the high side of C176 that is buffered by Q127/Q128. The resistor divider network of R315, R227, R229 and R232 provide the correct amount of compensation for stable operation and current limiting.

The output voltage is sampled by R215, R216 and R217 and sent to the inverting side of the error amplifier internal to the controller IC on U112, pin 1. Voltage loop compensation is set by C174, C175 and R221.

Sync pulse is added into the low side of C176 via C172 and R225. The free running frequency of the 15V converter (approximately 145 kHz) is set about 10% lower than the 26.5V converter. This longer duty cycle allows the sync circuit to synchronize the converter.

Over voltage is sensed using U116 as a reference and amplifier, CR129 acts as a crowbar on the output. Once the crowbar is turned on, opto-isolator U119 is activated to shutdown the power supply. The enable line must be toggled or AC voltage removed for 10 seconds to reset the power supply.

6.6.7 +5V CONVERTER

Operation of the +5V "Buck" DC/DC converter is the same as the +15V, except slop compensation is not required. Some values are different to get the 5.2V DC and current limit to 6A. The duty cycle is approximately 20%.

6.6.8 -5V CONVERTER

The -5V "Buck-Boost" converter scales and inverts the voltage. This converter is free running at approximately 75 kHz. The output switch and controller are built into the 5-leg TO-220 IC U114. L105 is the storage inductor. C204, R270 and R271 close the voltage feedback loop and are set for optimum stable transient response. C208/C209 reduce output ripple. Under-voltage protection is required on this stage and works the same as the over-voltage protection of the +15V and +5V buck converters, but has opposite polarity.

6.6.9 POWER SUPPLY REPAIR AND ALIGNMENT

If a power supply fails it is typically a Power MOSFET or Power Diode. In some cases the MOSFET gate may short and cause some of the driver circuits to be damaged. When replacing heat sunk components it is advisable to replace the sil-pad thermal interface material at the same time. The mounting hardware must be replaced exactly as built in the factory. The mounting screws for the power semiconductors MUST BE torqued to 4-5 in/lbs. Under torque and over torque can shorten the life of the semiconductor.

The majority of the voltage and current limits are set with fixed value components in the power supply. However, the +26.5V, +15V and +5.2V supplies are adjustable. When certain components are replaced, the voltages must be adjusted. The voltages should be set at light load (i.e. repeater in the Receive mode).

1. The +26.5V supply can be adjusted with R174 when any of the following components are replaced: R173, R174, R175, U109, U108, U102, R143, R170 or R171.

2. The +15V supply can be adjusted with R216 when any of the following components are replaced: R215, R216, R217 or U112.

3. The +5.2V supply can be adjusted with R254 when any of the following components are replaced: R253, R254, R255 or U113.

6.7 BATTERY BACK-UP MODULE

6.7.1 OPERATION

When a battery back-up module is installed in a power supply it performs the function of running a repeater in the absence of AC voltage. When AC is present it can be used to charge a pair of lead-acid batteries in series. The charger is a temperature compensated constant voltage charger. The maximum output current from the charger is 2.2A. The charger works when AC is present and the repeater is enabled. The charger switch on the battery back-up module must be "On". The temperature compensation thermal sensor is part of 023-2000-223 battery back-up module cable assembly.

When AC is low or not applied to the 023-2000-800 power supply the battery input takes over if the voltage is within range. The input voltage to the battery back-up module acts as the 26.5V supply and the other voltages in the power supply also are present, +15, +5.2 and -5V. When AC is restored, the battery back-up module disengages automatically. The change over from battery to AC or AC to battery may cause the repeater to reset, depending on battery condition and load status.

NOTE: When using a generator, the DC voltage must be between 23-28.5V (26.5V DC is recommended) and ripple voltage less than 1% or approximately 0.25V P-P.

6.7.2 CHARGER

The charger charges the batteries when the repeater is on and switch S101 is "on". A tap off of the main transformer of the power supply through wire W104 and a +26.5V line via wire W102 are what supply the charger with the necessary voltage to charge the batteries. The tap off of the transformer is biased by the +26.5V and then filtered through L101, C105 and C119. Since the tap from the power supply is not a regulated voltage, bleeder resistors R136/R137 dissipate some power when the batteries are fully charged. No load situation, the peak voltage of the tap is approximately 63V, is not impressed across the 50V capacitors C105/C119. During a battery charging condition the line voltage to the charger on U107, pin 2 should be about 35V.

While charging batteries, if the charge voltage is varied with respect to the temperature of the batteries, the lifetime of the batteries is increased dramatically. Figure 6-9 shows the algorithm used in float charge applications for two 12V lead-acid batteries in series. Figure 6-9 shows that the charge voltage should be 27.3V DC ±0.15V at 25°C (77°F) with -55 mV/°C temperature compensation.

An LM317M linear voltage regulator (U107) is used to create the temperature compensated charge voltage. This device is capable of delivering 2.2A of continuous current to the batteries.

To create a temperature compensated voltage an op amp (U104) is used as a voltage gain device from a temperature probe attached to the batteries (part of 023-2000-223). This op amp with R148/R149 defines the slope for the algorithm of Figure 6-9. The output of the temperature compensation is attached to the adjust pin of U107. R138-R140 allow the output voltage to be set properly at a given ambient temperature. F101 is a 4A resettable fuse used to prevent thermal run away in the event of U107 failure. If the output current to the batteries exceeds 4A this fuse opens. Once the current drops below 100 mA, the fuse closes automatically.

NOTE: If any of the charging components are replaced, R140 needs to be adjusted to set the output (battery back-up battery terminals) voltage to 27.3V ±0.15V when temperature sensor is at 22°C (71.6°F).

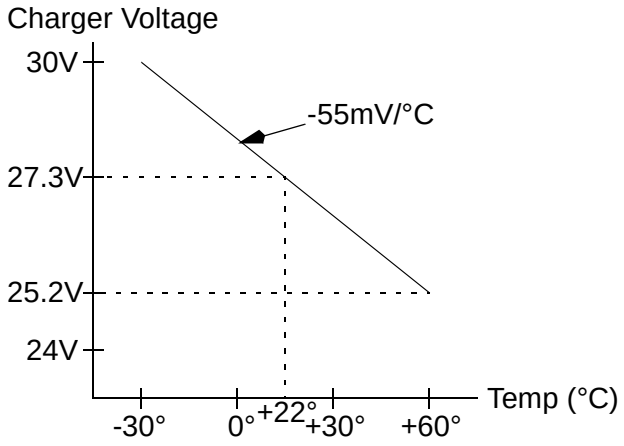


Figure 6-9 NO LOAD CHARGE VOLTAGE vs. TEMPERATURE

6.7.3 REVERSE BATTERY PROTECTION

To obtain reverse battery protection a number of techniques were implemented. Q108/Q110 are arranged in a Darlington configuration to isolate the output capacitors C109-C111 from conducting in the event the batteries are connected backwards. This circuit also provides a means to turn the battery charger off in case the user wants to run the repeater off of another DC source. S101 opens the base of Q105 which turns off Q104. CR111 is a green light emitting diode (LED) located on the right hand side of the battery back-up module when looking at the front of the power supply that tells the user the charger is in charge mode and is marked "On".

To notify the user that the batteries are connected improperly R101/CR101 are connected in series across the batteries. CR101 is a red LED that lights when the batteries are connected backwards and is located on the left hand side of the battery back-up module when looking at the front of the power supply. This LED is marked "Reverse Bat.". CR113 eliminates a path for the reverse battery current through the relay and over/under voltage protection circuitry.

NOTE: Exceeding -30V across the battery back-up terminals with the power supply on will destroy Q105.

6.7.4 ENGAGING THE RELAY

The main purpose of the Battery Back-Up Module (BBM) is that when the power supply loses AC line voltage, a pair of series connected 12V lead acid batteries (approximately 26.4V) or other 23-28.5V DC source will engage to the supply allowing the repeater to operate. To perform this function a voltage comparator (U101) is used to monitor the charge tap coming from the power supply.

A 2.5V reference voltage is supplied to the comparator from U102. The transformer tap voltage is smoothed and divided by CR114, C118, R116, R121 and R122. The values for these components were calculated so that when the AC line voltage is dropped to 70V AC, the output of the comparator turns Q103/ Q102 on which in turn engages the relay K101. The relay is capable of 30A which delivers the battery energy to the power supply via W102 with the return line being W103.

NOTE: When AC is restored, the relay disengages and the charger automatically begins to charge the batteries.

6.7.5 OVER/UNDERVOLTAGE SHUTDOWN

U101 is a quad comparator IC used to create the overvoltage and undervoltage shutdown circuitry. If the batteries are drained sufficiently enough such that the voltage of the batteries drops below 20.3V DC the output of the comparator goes low and turns Q102 off. By turning Q102 off the batteries are switched out of the circuit. The batteries cannot be switched back into the repeater until the voltage rises to 22.6V DC. This operation is in place to protect the repeater and the batteries. In the event the batteries are over charged, or the repeater is driven by the generator that has the voltage set too high, the relay will disengage above 30.5V DC. In order to switch the batteries back to the repeater, the voltage must drop below 29V DC.

In an overvoltage or undervoltage situation, whether AC is present or not, the red LED (CR105) lights until the problem is rectified. This light is located on the right-hand side of the battery back-up module when looking at the front of the power supply and is marked BAT-BAD.

6.7.6 BBM FAN CONTROL

The voltage supply to the thermal measurement circuit is taken from the 26.5V DC line into the BBM. A precision temperature sensor U106 is mounted on the PC board near a screw into the BBM bracket which transfers heat to the sensor. The output of this sensor is 10 mV/°C with a ±1% accuracy. This voltage is amplified by U105 with resistors R153/R154 setting the gain.

The output of this gain stage (pin 1) is fed to another gain stage that performs as a comparator. The output (pin 7) will go high when the heatsink temperature reaches 45°C and will go low when the temperature goes below 35°C. This output is sent to the power supply through Q106 to turn the fan on and off.

6.8 CARD RACK

The card rack provides slots for up to eight logic cards; including Main Processor Card (MPC), Main Audio Card (MAC) and the Interface Alarm Card (IAC). The IAC has a notch in the card to accommodate a pin in Slot-8 so that no other card can be plugged into this slot.

On the back of the card rack is the Backplane with plug-in connectors to the cards and cables to the RF modules, Power Supply and External Connector Board.

Refer to the component layout and schematic diagram in Section 10 for more information on the repeater backplane.

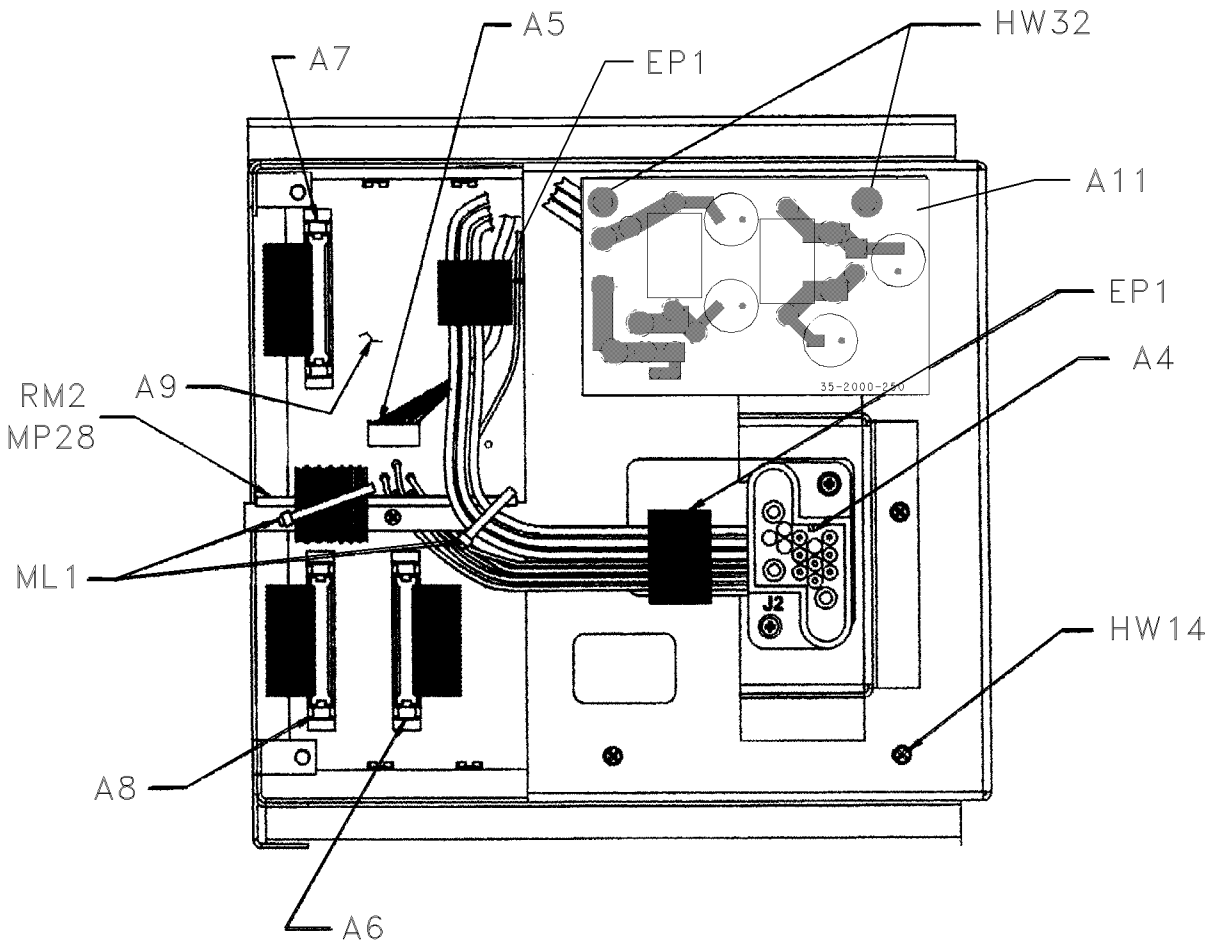


Figure 6-10 BACKPLANE CONNECTORS

6.9 EXTERNAL CONNECTOR BOARD

The external connector board (A10) is the interface for the alarm outputs, connecting repeaters through the high speed data bus.

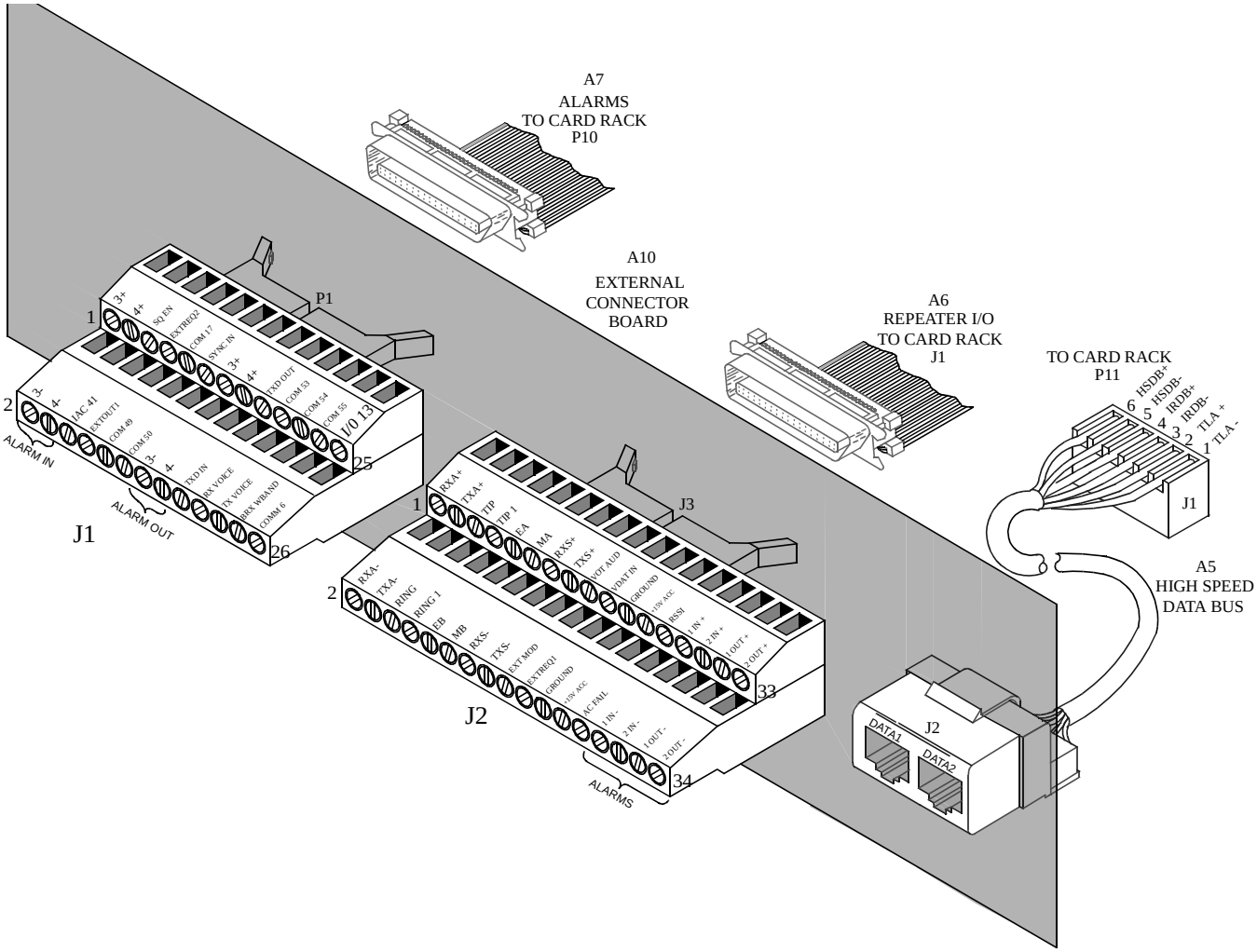


Figure 6-11 EXTERNAL CONNECTOR BOARD

6.10 MAIN PROCESSOR CARD

6.10.1 INTRODUCTION

The Main Processor Card (MPC) connects to the computer with repeater software to program the repeater parameters, sets and reads the alarms, handles communication between repeaters, maintains the audio gating for the MAC, handles initialization requests from cards and contains the repeater RF data for the Receiver, Exciter and CWID.

Control functions for each repeater are performed by the Main Processor in the MPC installed in each repeater. The MPC contains the main software and control over the repeater via microprocessor U27 (see Figure 6-17).

Information is exchanged between repeaters via a High-Speed Data Bus (HSDB) that interconnects all the MPCs. This control technique is called distributive processing and it eliminates the need for a separate system controller at each site. The HSDB processor (U13) on the MPC provides these control functions. The MPC also contains:

- Flash Memory, RAM, non-volatile EEPROM.
- I/O chip select to allow the addressing of data latches for Input/Output.
- Read/Write selection to be sent and received on the Controller Backplane.
- Clock line, data line and chip select line from the IAC to load the Receiver and Exciter synthesizers.
- Serial communication circuitry and processes for the High Speed Data Bus (HSDB).
- Asynchronous parallel communication to the other cards, i.e. alarm input and output circuitry.
- AC Power Failure indication from the IAC.
- Provides an output from the IAC to the power amplifier to control the output power.
- Exciter Logic Push-To-Talk (PTT).
- Receiver synthesizer lock, Exciter synthesizer lock, thermal level from the power amplifier, VSWR level from the PA, forward power level, RSSI signal level, audio levels from the MAC, Receiver and Exciter from the IAC.

6.10.2 MAIN CONTROLLER MICROPROCESSOR (U27)

This contains the main software and control over the repeater (see Figure 6-12).

The main controller (U27) is a VLSI (Very Large Scale Integration) CMOS 16-bit single chip computer with an 8-bit external data bus. This processor has software compatibility with the V20 (8086/8088), faster memory access, superior interrupt processing ability, and enhanced control of internal peripherals. This ROMless processor has a variety of on-chip components including 256 bytes of RAM, serial and parallel inputs/outputs, comparator port lines and timers.

Eight banks of registers are mapped into internal RAM below an additional 256-byte special function register (SFR) area that is used to control on-chip peripherals. Internal RAM and the SFR area are together and can be relocated anywhere in the 1M-byte address space. This maintains compatibility with existing system memory maps.

The two microprocessors and USART (U22) are reset by integrated circuit U17. Reset occurs when power is turned on, when the 5V supply drops below a threshold level or the reset switch (S1) is active.

When a microprocessor is reset, several internal registers are cleared and the program is started over from the beginning. Low-voltage reset prevents improper operation resulting from low-voltage conditions.

When power is turned on, the RESET output U17, pin 6 is initially high and the inverted RESET output U17, pin 5 is initially low. Once the 5V supply stabilizes, these outputs remain in these states for approximately 100 ms to ensure that resetoccurs. This time delay is set by capacitor C14 connected to U17, pin 3. If the 5V supply drops below a nominal level, the RESET outputs change states and microprocessor operation is interrupted until the 5V supply returns to normal. C3 prevents fast transients on the 5V supply from causing reset.

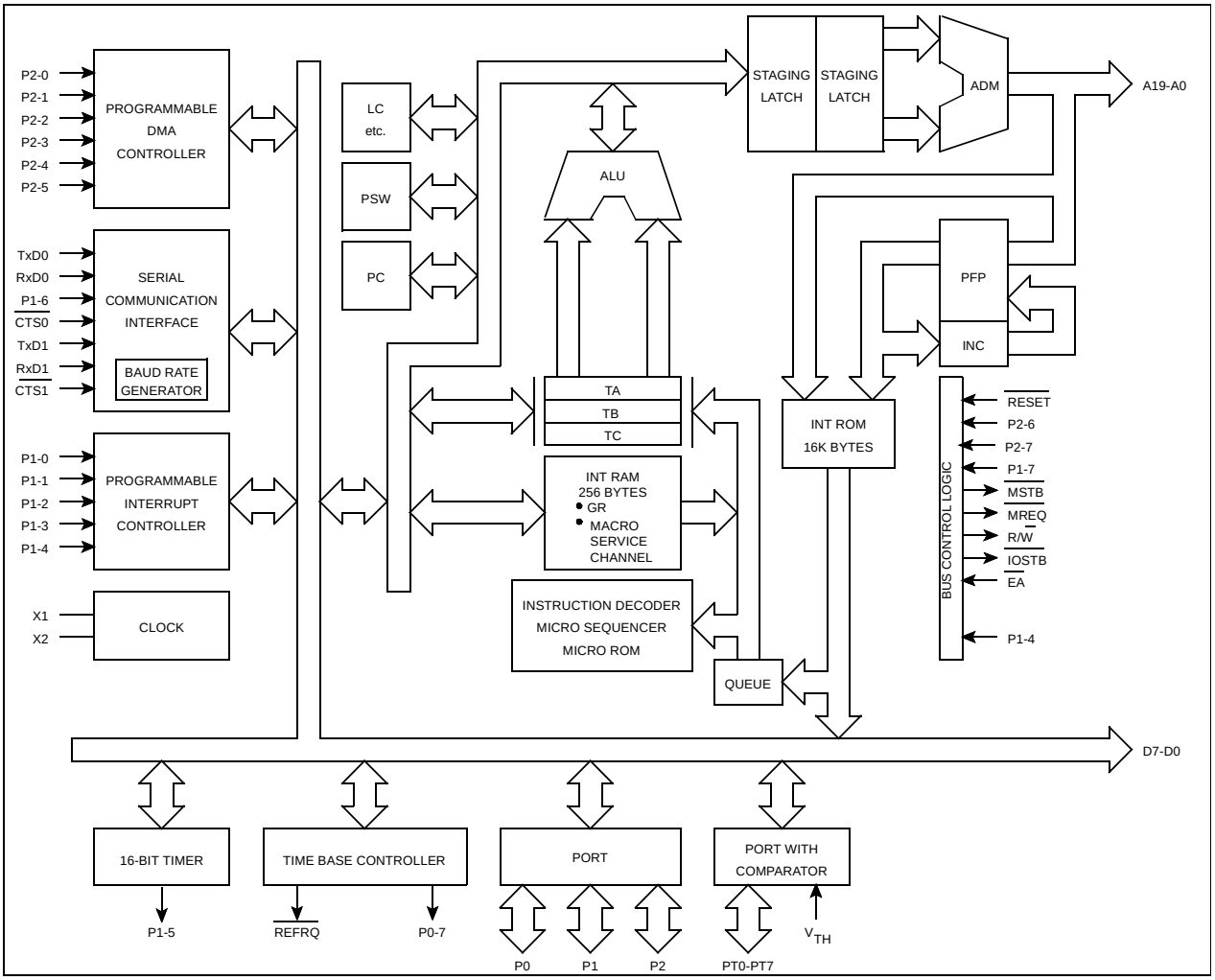


Figure 6-12 U27 BLOCK DIAGRAM

Manual reset can be accomplished by pressing push-button switch S1. When U17, pin 2 goes low, U17 goes into the reset sequence described.

6.10.3 HIGH SPEED DATA BUS MICROPROCESSOR (U13)

The HSDB processor (U13) on the MPC provides the interface with the HSDB. It monitors data on this bus and also transmits data on to this bus when necessary. Information on this bus indicates which repeaters are in use and also which mobiles are using the system. This information is used by the repeater to encode data messages to the mobiles that are monitoring that channel. These messages also include information on which repeater is free and current system priority.

Microprocessor U13 is an 8052 that uses external EPROM (Erasable Programmable Read Only Memory) U14, an 8-bit device that stores the program. The microprocessor uses 2k x 8 EPROM and 64k x 8 RAM. The RAM (Random Access Memory) is used for temporary data storage. The HSDB processor is configured by the Main Processor.

The internal data bus of the microprocessor has four input/output ports. These ports have eight lines each, giving a total of 32 input/output lines. These ports are designated P0, P1, P2, P3. P0 is used as a data bus. Ports P1 and P2 are always used as general purpose inputs/outputs. P3 is used for specialized functions, i.e. a serial port (RxD/TxD) and interrupt (INT).

The operating speed of the microprocessor is set by an 12 MHz clock generated by Y2. This clock frequency is divided down by an internal divider to provide a machine cycle time of 2.5 µs. Most program instructions are executed in one machine cycle and none require more than four machine cycles.

The microprocessor U13 communicates with the main processor (U27) through U9 and U10. U9 is a Transmit FIFO (First In First Out) and U10 is a Receive FIFO. This combination makes up an asynchronous parallel-to-parallel interface to the Main Processor.

Microprocessor U13 also calculates the current system priority for the channel. This priority is from the programming software responses and the current priority is sent to the main processor. U13 also reads repeater number and channel number information in memory. U13 also determines the current free repeater and includes that information in the data sent to the Main Processor.

6.10.4 CHIP SELECT DECODERS (U15/U4)

Selects the peripheral chip to read from or write to.

6.10.5 P1 SIGNAL CONNECTOR

The signal interface connector P1 (64 pin) that connects the Address and Data buses and control lines to the backplane connector.

Pins 1-10 ADDRESS BUS
Pins 33-42

Provides a path between the MPC main processor and the external memory on the MPC and the other cards in the Controller. This bus retrieves information programmed into memory for the operation of the repeater.

Pins 11-14 DATA BUS
Pins 43-46

Provides a means of transferring data to and from the CPU on the MPC, memory storage on each card and peripheral devices in and out of the MAC and IAC.

Pin 15 MREQ

A memory request line operates in conjunction with the Read/Write lines. These provide the ability to read from or write to the main processor memory on the MPC.

Pin 16 $\overline{\text{MSTB}}$

A memory strobe line used during MPC main processor Read/Write operations to external memory on the MPC and other cards plugged into the backplane.

Pin 17-20 UNUSED

Pin 21 LPTT

The Logic Push-To-Talk is an open collector from the Controller. It has a sink capability of 20 mA and a maximum voltage rating of 18V. The transmitter should produce power when this pin is a logic low. Transmit indicator is on the IAC and is controlled independently of the LPTT.

Pin 22-23 UNUSED

Pin 24/56 HSDB+/HSDB-

This interconnects all repeaters to provide an exchange of information. This control technique is called distributive processing and eliminates a separate system controller at each site. Information on this bus indicates which repeaters are in use and also which mobiles are using the system. This information is used by the repeater to encode data messages to the mobiles that are monitoring that channel. These messages also include information on which repeater is free and current system priority.

Pins 25-26 UNUSED

Pin 27/59 -5V IN

This is the -5V input to the MPC from the power supply via the Controller backplane.

Pins 28-29 +5V IN
Pins 60-61

This is the +5V input to the MPC from the power supply via the Controller backplane.

Pins 30/62 +15V IN

This is the +15V input to the MPC from the power supply via the Controller backplane.

Pins 31-32 GROUND
Pins 63-64

This is the ground connection to the MPC from the power supply via the Controller backplane.

Pin 47 READ

Used with the MREQ line to read data from the main processor and external memory.

Pin 48 WRITE

Used with the MREQ line to write data to the main processor and external memory.

Pins 49-55 UNUSED
Pins 57-58

6.10.6 J1 COMPUTER CONNECTOR

J1 is the MPC connection to the computer or modem.

Pin 1	Ground
Pin 2	Computer Tx
Pin 3	Computer Rx
Pin 4	Modem DCD

6.10.7 J2 MEMORY SELECT

J2 is jumpered to select either the Flash memory or the EPROM memory. Flash memory is ultra-fast data storage. The normal setting is pin 1 to pin 2.

Pin 1	+12V
Pin 2	U25, pin 1 Vpp
Pin 3	+5V

6.10.8 J3 BAUD RATE

J3 is jumpered to select the baud rate from the computer to the MPC, these two baud rates must be the same (see Figure 6-17). The baud rate of the computer can be found from the command line by requesting /b, /h or /? (see Section 6.10). To change jumper J13: Power off the station. Move P3 to the proper rate. Power on the station.

6.10.9 S2/S3 HSDB SETTINGS

These switches configure; the HSDB for RS-485 or single-ended 5V operation, indicate if the Summit repeaters are connected to existing repeaters or only Summit repeaters, and if the repeater is an end repeater termination. Refer to Sections 2.9 and 7.5.8.

6.10.10 J4 EPROM MEMORY LOADING

This jumper selects EPROM memory loading for LTR systems. The LTR setting is pin 3 to pin 4.

6.10.11 J5 HSDB SPEED

J5 is jumpered to select the data bus speed. J5, pins 2/3 select the LTR 12 MHz crystal.

6.10.12 J6 WATCHDOG

This jumper enables or disables the watchdog timer for reset. Normal operating mode is P6 jumpering J6, pins 2/3. This jumper should not be moved or removed.

6.11 MAIN AUDIO CARD

6.11.1 INTRODUCTION

This control card stores the information required to operate the routing of audio and data from the inputs of the repeater to the outputs. Data is received on the address bus from the MPC for the operations to perform. The Audio/Data microprocessor and the latches open and close gates to route a path for the audio or data.

Audio control functions for each repeater are performed by the Main Processor in the MPC. The MPC contains the software and maintains control over the repeater via microprocessor U27. The audio/data microprocessor passes received data to the main processor, and it is given the programmable parameters for the gates.

Information is exchanged between the cards in the Controller Backplane via a data bus and an address bus. The address bus provides the link between the main processor and the chip and the address latches on the MAC. These latches control the octal latches that select the audio and data gates. The data bus is the link between the Main Processor and the Audio/Data Processor on the MAC. The Main Processor controls the data to the octal latches and opens and closes the gates required to route audio/data in and out of the repeater. The MAC also contains:

- The audio interface between the receiver and exciter and to the external connections.
- The receive audio filtering with de-emphasis.
- The squelch filter and detector.
- Slow decay timing circuit that controls a mute gate on the main receive audio.
- A filter, DC restoration and slicer circuitry for detecting the subaudible data.
- The fast squelch and data fed to the microprocessor that decodes the data and uses the squelch line as a data qualification signal.
- Transmit audio filter and limiter with pre-emphasis.

6.11.2 AUDIO/DATA MICROPROCESSOR (U111)

This Audio/Data microprocessor is on the MAC card and is used to decode LTR data received from the mobiles. The LTR data is applied to U111, pin 8 (P1.7 input). When a word is successfully decoded the data is then sent to U161 (Tx FIFO) and transmitted on the data bus in parallel to the main processor on the MPC.

When it is time to transmit the CW Identification, the main processor on the MPC sends the identification to U111 via the data bus and U160 (Rx FIFO). The CWID is sent to the Tx Data Amplifier and Filter. The output of the filter is summed with the transmit audio and sent to the Exciter.

U111 also uses six octal latches to provide additional input and output lines. Latch U107/U108 provide outputs which allow U111 to control various audio gates. These gates control the CWID, FSK data, and receive/transmit audio signals.

Latch U106 provides outputs which allow U111 to route signals to the Audio/Data Test Point by switching gates on and off. U106 also provides adjustment of the selected EEPOTs.

U155-U156 allow U111 to select the EEPOT to adjust with chip select lines. These latches also provide routing of some audio/data signals through gates.

In addition, U111 controls the receive and transmit audio gates, receiver squelch, several front-panel indicators, and other functions. U111 encodes the data messages transmitted to mobiles monitoring that channel, and controls transmitter keying.

6.11.3 RECEIVE AUDIO

The Receive Wide Band Audio (RX WBAND) signal from the Receiver is fed into the MAC on P100, pin 27. This audio signal includes; audio, LTR data, and noise. The audio processing circuit provides filtering and amplification of the audio signal before it is routed to the outputs on the MAC card.

A low-pass filter consisting of U121A/B attenuates frequencies above 3 kHz. This removes high-frequency noise from the audio signal. From the filter the signal is fed to amplifier U122A to increase the level before the high-pass filter to preserve adequate hum and noise ratio.

From the audio amplifier the signal is fed to a high-pass filter consisting of U122B/C/D. This filter attenuates frequencies below 300 Hz which removes data present in the wide band audio signal. These filters are configured to act like large inductors. The signal is then fed to U163A which provides 6 dB per octave de-emphasis.

Audio gates U113B/C/D permit noise squelch circuit, control logic, and audio switch to control gating of the audio signal. The control signal from the noise squelch circuit is applied to U113B through U113D. When a carrier is detected, this input is high and U113B passes the signal. Programming determines the gating of audio. When audio is passed by U113B/C and U114A, the audio can be routed through other gates to various outputs (see Section 6.11.6).

6.11.4 RECEIVE SQUELCH CIRCUITRY

The receive wide band audio includes audio, data and noise. The squelch circuit detects this noise to determine receive signal strength. When no carrier or a weak carrier is received, there is a large amount of noise present. Conversely, when a strong carrier is present, there is very little noise present.

U135A is a high-pass filter which attenuates frequencies below approximately 30 kHz so that only high-frequency noise is passed. This noise is amplified by U135B and U123A. A level control adjusts the gain of amplifier U135B. The gain of U123A is partially set by a thermistor to compensate for circuit gain and noise level changes caused by temperature variations.

The amplified noise is then applied to a bridge rectifier. The difference between bridge rectifier outputs is applied to the inputs of U123B. The output of U123B is positive-going pulses. These pulses are applied to U123C which is a Schmitt trigger. When the input signal rises above the reference the output goes low and causes the reference voltage to decrease slightly adding hysteresis to the triggering level. This hysteresis prevents intermittent squelching when the receive signal strength is near the threshold level.

The output of U123C is applied to U123D and Logic Squelch to Audio/Data Gate U159B and audio/data processor U111. Gate U159B routes the squelch output to the Audio/Data Test Point J100. U123D functions as a timing buffer. The output of U123D is applied to Receive Squelch Active Gate U113D. When this gate is closed, the squelch circuit controls Normal Receive Gate U113B to block receive audio if no signal is present.

6.11.5 RECEIVE DATA CIRCUITRY

The receive wide band audio signal is the unfiltered output of discriminator U202 in the Receiver. Therefore, this signal contains audio, LTR data, and noise. A low-pass filter formed by U124A/B attenuates frequencies above 150 Hz by 24 dB per octave so that only the data frequencies are passed. From the filter the signal is fed to amplifier U125A. The gain of U125A is adjusted by a level control. The output of U125A can be routed through Data To Audio/Date Gate U159C and the Audio/Data Test Point J100.

DC restoration circuit converts the data signal from AC floating near ground to a digital signal at levels of 0 and 4.5V. U125B/C provide the reference voltage on the inverting input of comparator U125D. Positive peak detector U125B handles the positive-going peaks of the data signal. Negative peak detector U125C handles the negative-going peaks of the data signal.

The voltage on non-inverting input to U125D is midway between the positive- and negative-going peaks. The data input is on the non-inverting input of U125D. When the data signal rises above the reference voltage, the output goes high. Conversely, when the input voltage drops below the reference voltage, the output goes low. The receive data is then passed to audio/data processor U111.

6.11.6 RECEIVE AUDIO PROCESSING

The receive audio signal is fed into the MAC on P100, pin 27. When a mobile-to-mobile call is received, Repeat Gate U153C is enabled and the receive audio signal is routed through Transmit Option Gate U158C to the input of the transmit audio buffer U164B to be retransmitted. Repeat Gate U153C is controlled by processor U111 through latch U107. A logic 1 on the control input causes the signal to be passed.

When the received audio must be routed to the backplane (i.e. for other cards), Receive Voice Gate U115B is enabled by processor U111/latch U108 and passes the audio signal to amplifier U120B. Receive To Backplane (RX TO BP) U115C is enabled and passes the amplified audio to the backplane.

When the audio received must be routed to the external speaker or speaker/microphone, Local Audio Mute Gate U114D is enabled by U111/latch U108. The audio is passed to local audio output amplifier U132. The gain of U132 is adjusted by the local audio volume control and on/off switch.

6.11.7 VOTER AUDIO

When used, the Receive audio from the voter receiver comes into the MAC on P100, pin 25. Amplifier U120A sets the gain of the signal and the output is routed to Voter Audio Mute Gate U115A. The gate is controlled by A/D processor U111/latch U108. If the gate is enabled, the audio goes to the Receive Mute Gate U113C and passes throughout the MAC Card.

6.11.8 COMPANDOR OPTION

The compandor option enhances the receive and transmit audio when used in conjunction with the Telephone Interface Card (TIC) in LTR systems.

The filtered Receive Audio passes through the Receive Mute Gate U113C to the expander input on A301, pin 1. The expand output of A301, pin 2 is coupled to the audio outputs by U114C.

The TX-VOICE from P100, pin 32, passes through TX Voice Gate U158A to the expander input on A301, pin 5. The compressed output of A301, pin 4 is passed to the TX Audio Buffer.

6.11.9 TRANSMIT AUDIO

PTT switch (Q101/Q102) provides local microphone Push-To-Talk (PTT) indication to U105. U105 then tells U111 via the data bus that the local microphone PTT has been activated.

U164A amplifies the microphone audio signal to provide the correct input level to U164B. Local Microphone Mute Gate U117C is controlled by A/D processor U111/latch 106. The function of U117C is to mute the local microphone audio when the local microphone PTT switch is pressed. This prevents interference if the microphone remains live when the PTT switch is pressed.

Buffer U164B combines the microphone audio signal from U164A with the audio signal from the Repeat Gate U153C.

U127B/C form a high-pass filter that attenuates frequencies below 300 Hz to prevent interference with the LTR data applied at U129B. Pre-emphasis at 6 dB per octave is provided by an RC combination before the signal is fed to the Limiter U127D.

Limiter U127D and rectifiers form a precision limiter which prevents over modulation caused by high-level input signals. With normal input levels, the output of a bridge rectifier follows the input of the bridge. When a high-level signal is applied to the bridge, the bridge opens and the output of the bridge is limited to a specific level.

The output of the limiter passes to a composite 6-pole splatter filter formed by U127A, U128D and U128A separated by buffers U128B and U128C.

The output from U128A is fed to Normal Modulation Mute Gate U118B that is controlled by A/D processor U111/latch U106. When enabled, the gate passes transmit audio to EEPOT U149. U149 is an electronically adjustable potentiometer that adjusts the gain of transmit audio amplifier U129C. The gain of U129C can only be adjusted through the software. Therefore, a computer must be attached to the MAC card when levels are set.

The output of U129C is fed to summing amplifier U129B where it is combined with LTR transmit data and CWID when present. The gain of audio and data are the same so unity gain is produced. The output signal is fed to the TCXO where it frequency modulates the transmit signal.

6.11.10 TRANSMIT AUDIO PROCESSING

Transmit voice from the backplane comes into the MAC on P100, pin 32. When used this signal passes to the transmit voice amplifier U130A. The output level of the amplifier is adjusted by a level control. The output of U130A is applied to another transmit voice amplifier U130B and Transmit Voice Gate U158A. U158A is controlled by A/D processor U111/latch U107. When enabled, the gate passes the voice to Transmit Option Gate U158C and on to the transmit

audio buffer U164B. Transmit Voice amplifier U130B is adjusted by a level control. The output is fed to Transmit Net Gate U153B. Gate U153B is controlled by A/D processor U111/latch U155.

6.11.11 TRANSMIT DATA AND CWID PROCESSING

The data signal is produced by A/D processor U111 on Transmit Data and Transmit Shape outputs. The transmit shape output is normally the opposite logic level of the transmit data output when data is transmitted. However, the bit before a logic transition occurs, the transmit shape output is the same logic level as the transmit data output. This results in a logic 1 level that is slightly higher and a logic 0 that is slightly lower. This pulse shaping minimizes interference between data bits when the data is filtered by the low-pass filter.

The data from U111 is fed to buffer U126A and Transmit Data Enable Gate U117B. Gate U117B is controlled by A/D processor U111 directly. When enabled this gate passes the data to EEPOT U151. U151 is an electronically adjustable potentiometer that adjusts the gain of transmit audio amplifier U126B. The gain of U126B can only be adjusted through the software. Therefore, a computer must be attached to the MAC card. U126B provides the required signal level at the output of the low-pass filter. A relatively stable DC bias voltage for U126C/D is required because these stages are DC coupled to the transmit TCXO (see Section 6.2.2) and changes in bias voltage can cause fluctuations in the transmit frequency.

U126C/D form a low-pass filter that attenuates square-wave harmonics in the data signal above 150 Hz to prevent interference with the audio band. From this filter the signal is fed to summing amplifier U129B and combined with the transmit audio signal. The output of U129B is fed to Transmit Modulation Mute Gate U118D. This gate is controlled by A/D processor U111/latch U106. When enabled, transmit audio and data are passed to the Exciter modulation input and the transmit TCXO.

When needed the External Modulation input on P100, pin 11 is fed to External Modulation Mute Gate U118C. Gate U118C is controlled by A/D processor U111/latch U106. When enabled, this gate passes the modulation on pin 11 to the summing amplifier U129B and gate U118D to the modulation input of the Exciter.

The repeater on the lowest frequency channel in each system must periodically transmit the station call letters as a continuous-wave identification encoded by Morse Code. This identification is programmed with the Edit Parameters software.

The CWID output is controlled by A/D processor U111/latch U107. This output is fed to CWID tone generator U100B/A and turns the tone generator on and off to create the Morse Code. From the tone generator the signal is fed to bandpass filter U129A. This filter passes the 800 Hz fundamental present in the signal. The output of the filter is jumpered by P106 on J106, pins 2/3 and P107 on J106, pins 4/5 to the summing amplifier and applied to gate U118D, and to the modulation input of the Exciter.

The input and output connectors for the MAC are defined as follows.

6.11.12 P101 SIGNALING CONNECTOR

The signal interface connector P101 (64 pin) connects the Address and Data buses and control lines to the backplane connector. See Figures 6-18 and 6-19.

Pins 1-10 ADDRESS BUS
Pins 33-42

This provides a path between the MPC main processor and the processor and memory of the MAC. This bus retrieves information programmed into memory for the operation of the MAC.

Pins 11-14 DATA BUS
Pins 43-46

This data bus provides a means of transferring data to and from the processor on the MAC with peripheral devices in the MAC.

Pin 15 MREQ

A memory request line operates in conjunction with the Read/Write lines. These provide the ability to read from or write to the processor memory.

Pin 16 $\overline{\text{MSTB}}$

The memory strobe line is used for MAC processor Read/Write operations to external memory.

Pin 17-20 UNUSED

Pin 21 LPTT

The Logic Push-To-Talk is not used.

Pin 22-23 UNUSED

Pins 24/56 HSDB +/-

The High Speed Data Bus interconnects the Viking VX repeaters. A 50 ohm termination is required if Viking VX repeaters are used with existing repeaters and the interface.

Pins 25/57 UNUSED

Pin 26 TLA DB

The Trunk Line Accounting Data Bus is used for telephone interconnect calls.

Pin 27/59 -5V IN

This is the -5V input to the MPC from the power supply via the Controller backplane.

Pins 28-29 +5V IN
Pins 60-61

This is the +5V input to the MPC from the power supply via the Controller backplane.

Pins 30/62 +15V IN

This is the +15V input to the MPC from the power supply via the Controller backplane.

Pins 31-32 GROUND
Pins 63-64

This is the ground connection to the MPC from the power supply via the Controller backplane.

Pin 47 READ

Read is used with the MREQ line to read data from the processor and external memory.

Pin 48 WRITE

Write is used with the MREQ line to write data to the processor and external memory.

Pins 49-55 UNUSED

Pin 58 VOTER DATA IN

This is used in a Voter system. Data from the voter site is injected at this pin.

6.11.13 P100 EXTERNAL OUTPUTS

Connector P100 contains the audio and data outputs to the terminal block on the back of the Repeater cabinet. These outputs are connected to other external devices. The input and output connectors for the connector are defined as follows.

Pins 1-6 UNUSED

Pin 7 3.5V

This is the 3.5V DC TCXO reference voltage from the Exciter to the MAC.

Pin 8 TX DATA OUT

This output contains trunking signaling data and CWID data when enabled at jumper J106 and used with external optional equipment.

Pin 9 TX DATA IN

This input would normally contain trunking signaling data, CWID data, and an externally summed in signal. This input is enabled at J106 and is used with external optional equipment.

Pin 10 EXT REQ1

This input provides for external requests from optional equipment.

Pin 11 EXT MOD

This input provides for external wide band modulation of the Exciter with out any filtering. This input is not used at this time.

Pins 13-26 UNUSED

Pin 27 RX WB AUDIO

The Receive Wide Band Audio from the Receiver audio demodulator through the RF Interface Board. The typical amplitude is 387 mV RMS (-6 dBm) and 2V DC with Standard TIA Test Modulation into the receiver.

Pin 28 A D LEVEL

This is the Audio/Data Level output.

Pin 29 TX MOD

The output of this pin is produced by audio and data inputs to the Repeater to produce the signals on this pin. This signal goes through the RFIB and then to the Exciter.

Pin 30 UNUSED

Pin 31 RX VOICE

This is receive audio output connected to the backplane.

Pin 32 TX VOICE

This is transmit audio input connected to the repeat gate.

6.11.14 J100 A D LEVEL TEST POINT

This test point located on the front card edge is used during alignment to monitor audio and data.

6.11.15 J101 SPEAKER/MICROPHONE

This jack is used in conjunction with J102 when a combination speaker/microphone is used during setup and testing of the repeater.

6.11.16 J102 LOCAL MICROPHONE

This jack is used for a microphone to key the Exciter and inject transmit audio.

6.11.17 J103 GROUND

This jack provides a ground connection for the MAC when monitoring the test points.

6.11.18 J104 EXTERNAL SPEAKER

This provides an external speaker connection at the repeater site for monitoring.

6.11.19 J105 WATCH DOG

J105 enables or disables the watchdog timer for reset. Normal operating mode is P105 jumpering J105, pins 2/3. This jumper should not be moved or removed.

6.11.20 J106 TX DATA PATH

Jumpers P106/P107 connect J106, pins 1-2/3-4 for external options that require the Tx Data signal. Normal operation connects J106, pins 2-3/4-5.

6.11.21 A301 COMPANDOR CONNECTIONS

EP101	Expand In
EP102	Expand Out
EP103	Ground
EP104	Compress Out
EP105	Compress IN
EP106	+5V

6.12 INTERFACE ALARM CARD

This card utilizes the information required to operate the alarms designated in the programming of the repeater. Data is received on the address bus from the MPC for the; operation to perform, the processor and external memory, open and close relays on the outputs, and receive alarm indications on the inputs. This information is either routed to external devices or alarm outputs can be wired to alarm inputs (see Figure 4-10).

The Interface Alarm Card (IAC) contains 4-input contacts and 4-output contacts. The 4- inputs can be disabled, energized or de-energized. The 4-output relays are dry contacts that have a 2A rating and can be either normally open or normally closed.

The electromechanical relay outputs are comprised of eight SPDT (normally open) relays. The relays are all open at power-on. Data to the relay is latched by a write to the base address.

The IAC activates relays when alarm trigger events occur. The IAC monitors for alarm activity in the system and can set the various output relays as defined by the user during programming. When an external alarm is set it can be monitored from a remote location. Refer to Section 4.3.3 for alarm programming.

6.12.1 RELAY OUTPUTS

The alarm relay outputs are provided via a terminal block on the back of the repeater (see Figures 6-13 and 6-14).

The alarm outputs are on the terminal block at the rear of the repeater.

6.12.2 ISOLATED INPUTS

The isolated alarm inputs are provided via a terminal block on the back of the repeater (see Figures 6-13 and 6-14).

The isolated inputs are driven by either AC or DC signals. The active high inputs can be set by switches to be polarity sensitive, non-polarity sensitive or add a resistance in series to dissipate unused power (see Figure 6-15).

The active low inputs can also be set for either +5V or +15V operation when a ground closure is required to provide an active alarm.

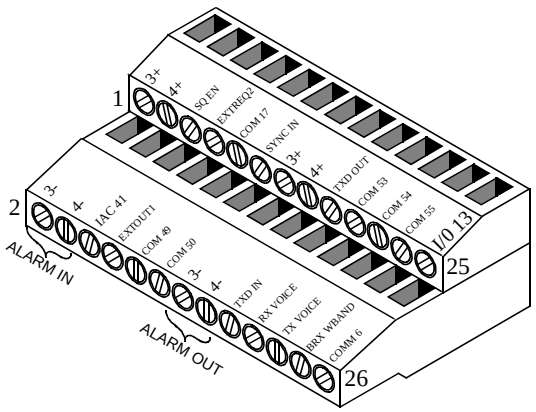


Figure 6-13 4 I/O J1 ALARM OUTPUTS

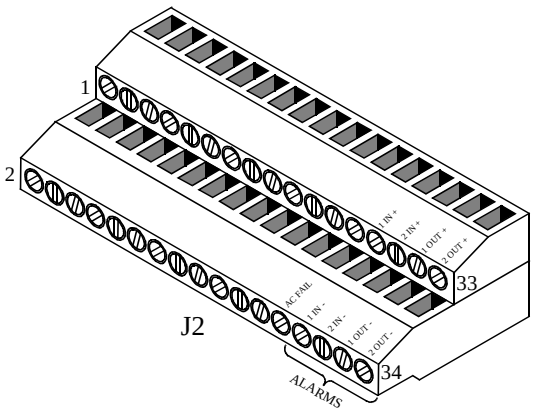


Figure 6-14 4 I/O J2 ALARM OUTPUTS

Standard 12V/24V AC control transformer outputs can be accepted as well as DC voltages. This input voltage range is 5-24V RMS. External resistors connected in series may be used to extend the input voltage range.

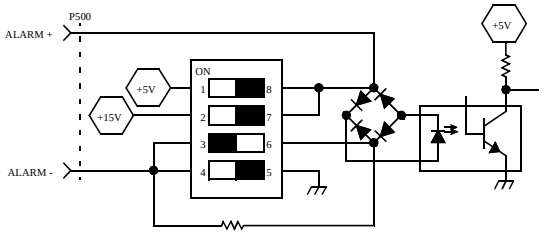


Figure 6-15 S500-S503

6.12.3 ALARM INDICATORS

There are three forms of alarm indicators from the repeater. One form is the two red LEDs and display combination on the MPC. Refer to Table 1-2 for the combinations and definitions of the active alarms.

Another form is the output relay to the terminal blocks at the rear of the repeater where outputs can be wired to external devices or to alarm inputs.

The third form is the output relay and to transmit a 15-character description of the alarm over-the-air to a remote location. The description is sent in Morse code with a transmit ID assigned during programming. A transceiver programmed with this ID can monitor the repeater and alert the system owner when an alarm occurs.

6.12.4 ALARM FUNCTIONS

The alarms can be configured in various modes to alert the system owner to conditions and hazards with the equipment and the repeater site facility. A few of the possibilities are shown in Figure 6-16. In this example the input alarm 2 of Repeater 1 is connected to the door of the building, input alarm 3 of Repeater 5 is connected to the fire alarm system, the AC fail alarm (#16 see Table 1-2) is mapped to alarm 2 output so it can be transmitted (see Figure 4-10) and the output alarm 1 of Repeater 1 is connected to the input alarm 1 of Repeater 2 and so on until the output alarm 1 is fed back to the input alarm 1 of Repeater 1. Then the RF Shutdown alarm (#32) is mapped for alarm 1 in each repeater. This configuration allows Repeater 2 to give an alarm when Repeater 1 has an RF Shutdown alarm output, etc.

The input alarms are given a 15-character description during programming and a Transmit ID. These are used when an input alarm is activated to send a Morse code message consisting of the description over the air to a monitoring transceiver programmed with this ID.

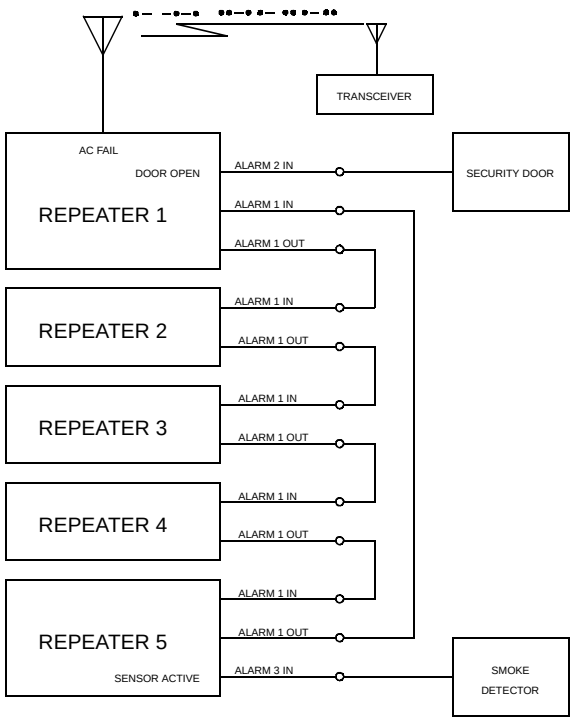


Figure 6-16 ALARM EXAMPLE

There are 40 internal alarms that can be included in the output alarm configuration (see Table 1-2). These alarms can also be programmed to send an output as shown in the cross reference screen of the alarm configuration menu (see Figure 4-10). Among these alarms are the thermal sense from the PA and the AC fail alarm output on the terminal block at the rear of the repeater to activate the battery backup.

6.12.5 P500 SIGNALING CONNECTOR

The input and output connectors for the IAC are defined as follows. The signal interface connector P500 (64 pin) connects the Address and Data buses and control lines to the backplane connector. See Figure 6-20.

Pins 1-4 ADDRESS BUS (A12-A19 Only)
Pins 33-36

This address bus provides a path between the MPC main processor and the latches and multiplexers of the IAC. This bus retrieves information programmed into the MPC memory for the operation of the IAC.

Pins 5/37 ALARM 1 IN +/ALARM 1 IN -

This is an input received from a connection to an external device as a specific alert condition.

Pins 6/38 ALARM 2 IN +/ALARM 2 IN -

This is an input received from a connection to an external device as a specific alert condition.

Pins 7/39 ALARM 3 IN +/ALARM 3 IN -

This is an input received from a connection to an external device as a specific condition.

Pins 8/40 ALARM 4 IN +/ALARM 4 IN -

This is an input received from a connection to an external device as a specific alert condition.

Pin 9 SQUELCH ENABLE

This is an output to rear connector J1. It can be configured for inverted output, non-inverted output or logic controlled non-inverted output.

Pin 10 EXTERNAL REQ 2

This is an input received from a connection to an external device.

Pins 11-14 DATA BUS
Pins 43-46

This data bus provides a means of transferring data to and from the latches and multiplexers on the IAC with peripheral devices in the IAC.

Pin 15 MREQ

A memory request line operates in conjunction with the Read/Write lines. These lines read from or write to the MPC processor memory.

Pins 16/17 UNUSED

Pin 18 SYNC IN

This is an input received from a connection to an external device.

Pins 19/51 ALARM 1 OUT +/ALARM 1 OUT -

This is an output to an external device to perform a specific function.

Pins 20/52 ALARM 2 OUT +/ALARM 2 OUT -

This is an output to an external device to perform a specific function.

Pins 21-23 UNUSED

Pins 24/25 +15V ACCESSORY

This DC supply is an output to an external device through rear connector J1.

Pins 26/58 +15V FILTERED

This DC supply is an output to an external device through rear connector J1.

Pins 27/59 -5V IN

This is the -5V input from the power supply via the Controller backplane

Pins 28-29 +5V IN
Pins 60-61

This is the +5V input to the MPC from the power supply via the Controller backplane.

Pins 30/62 +15V IN

This is the +15V input to the MPC from the power supply via the Controller backplane.

Pins 31-32 GROUND
Pins 63-64

This is the ground connection to the MPC from the power supply via the Controller backplane.

Pins 41-42 UNUSED

Pin 47 READ

Read is used with the MREQ line to read data from the MPC processor and external memory.

Pin 48 WRITE

Write is used with the MREQ line to write data to the MPC processor and external memory.

Pins 49-50 UNUSED

Pins 53-55 UNUSED

Pin 56 THERMAL SENSOR

The Thermal Sensor monitors the PA temperature and creates an alarm condition if the temperature exceeds the limit.

Pin 57 POWER SWITCH

Pin 57 turns the voltage from the power supply to the Repeater on and off. This pin is connected to the on/off toggle switch S508.

6.12.6 P501 EXTERNAL OUTPUTS

Connector P501 contains data and control outputs to the terminal block on the back of the Repeater cabinet. These outputs are connected to other external devices.

The input and output connectors for the connector are defined as follows.

Pins 1/17 ALARM 3 OUT +/ALARM 3 OUT -

Pins 2/18 ALARM 4 OUT +/ALARM 4 OUT -

These are outputs to external devices to perform a specific function.

Pin 3 RX WBAND

Receive Wide Band Audio from the Receiver audio demodulator through the RF Interface Board. The typical amplitude is 387 mV RMS (-6 dBm) and 2V DC with Standard TIA Test Modulation into the receiver.

Pins 4-6 UNUSED

Pin 7 EXT OUT 1

This is an external output to rear connector J1.

Pin 8 RF CLOCK

The clock will control the synthesizer chips and power control circuit when loading. This pin is a TTL input from the Controller.

Pin 9 AC FAIL IN

This input from the AC supply is used by the AC fail output to indicate that the AC has been interrupted.

Pin 10 SYN CS RX

This is the chip select pin for the main receiver synthesizer chip. This chip is the same part as used in the Exciter. A low loads the synthesizer.

Pin 11 UNUSED

Pin 12 RF MUX 1 INH

The Multiplexer-1 Inhibit (U105, pin 6) is a CMOS input from the Controller that inhibits (disables) the Multiplexer-1 output with a logic high.

Pin 13 RF MUX 2 INH

The Multiplexer-2 Inhibit (U106, pin 6) is a CMOS input from the Controller that inhibits (disables) the Multiplexer-2 output with a logic high.

Pin 14 RF MUX 3 INH

The Multiplexer-3 Inhibit (U104, pin 6) is a CMOS input from the Controller that inhibits (disables) the output from the RF 3 Multiplexer with a logic high.

Pin 15 PC STR

The Power Control Strobe is normally low until after the power control data is shifted into the power control register. Then the strobe line goes high and back to low. The clock or data lines cannot be changed until after the strobe is set.

Pin 16 HS CS EX

This is the Exciter high stability synthesizer chip select. A low enables loading the high stability synthesizer loop. This pin is only used on high stability equipped units.

Pins 19-21 UNUSED

Pin 22 BUF RX WBAND

This is buffered Receive Wide Band Audio from the receiver audio demodulator through the RF Interface Board. The typical amplitude is 387 mV RMS (-6 dBm) and 5V DC with Standard TIA Test Modulation into the receiver. This is an output to the rear connector J1.

Pin 23 AC FAIL OUT

This is an indication that the AC power has been interrupted.

Pin 24 UNUSED

Pin 25 HS CS RX

This is the receiver high stability synthesizer chip select. A low enables loading the high stability synthesizer loop. This pin is only used on high stability equipped units.

Pin 26 SYN CS EX

Pin 26 is the exciter main Synthesizer Chip Select that allows input of data to U403 when the line is pulled to logic low.

Pin 27 UNUSED

Pin 28 A D LEVEL

20 lines (of the possible 24) of RF functions sampled are multiplexed to the Controller through this pin using three multiplex chips.

Pin 29 RF DATA A

Data A (U105, pin 11) is the least significant bit (LSB) in the 3 multiplex chips located on the RFIB. This pin is a CMOS input from the Controller requiring a logic high for activation.

Pin 30 RF DATA B

Data B (U105, pin 10) is the middle significant bit in the 3 multiplex chips located on the RFIB. This pin is a CMOS input from the Controller requiring a logic high for activation.

Pin 31 RF DATA C

Data C (U105, pin 9) is the most significant bit (MSB) in the 3 multiplex chips located on the RFIB. This pin is a CMOS input from the Controller requiring a logic high for activation.

Pin 32 RF DATA

This is a data pin with TTL levels from the Controller which has the dual role of loading the synthesizer chips and adjusting the power control D/A lines for proper output power. Up to four synthesizer chips and a shift-register could be connected to this pin.

6.12.7 J500 A D LEVEL TEST POINT

20 lines (of the possible 24) of RF functions sampled are multiplexed to the Controller through this pin using three multiplex chips.

6.12.8 J501 GROUND

J501 is an IAC ground reference for test points.

6.12.9 J502 +15V

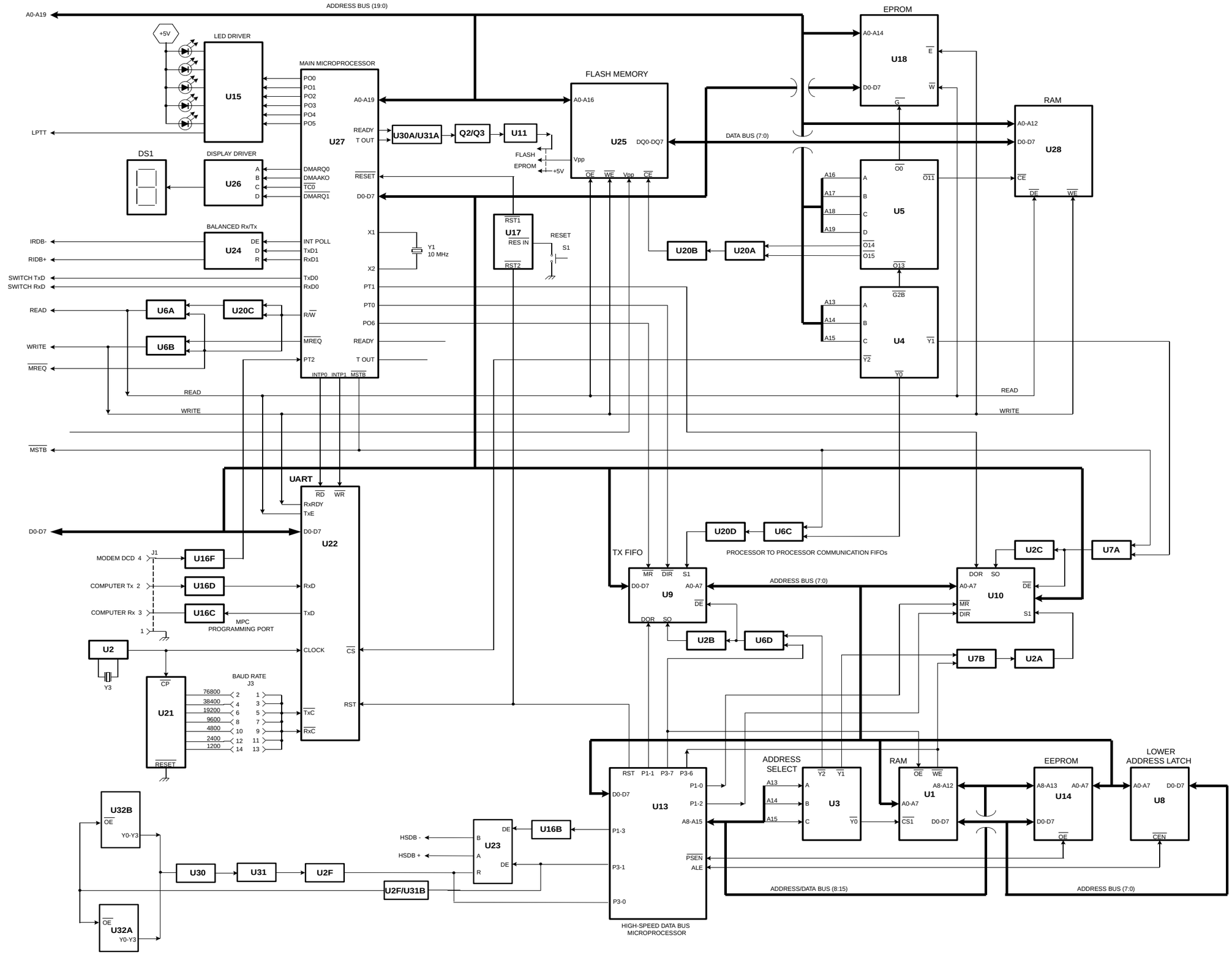
J502 is a voltage test point.

6.12.10 POWER SWITCH

S508 turns the power supply DC voltage on and off from the front of the IAC.

6.12.11 J505 SQUELCH ENABLE OUTPUT

P505 jumpers J505, pins 1/2 to configure the squelch enable output for an inverted output. P505 jumpers J505, pins 2/3 to configure the squelch enable output for a non-inverted output. P505 jumpers J505, pins 3/4 to configure the squelch enable output for a non-inverted output under the control of U503.



May 1998
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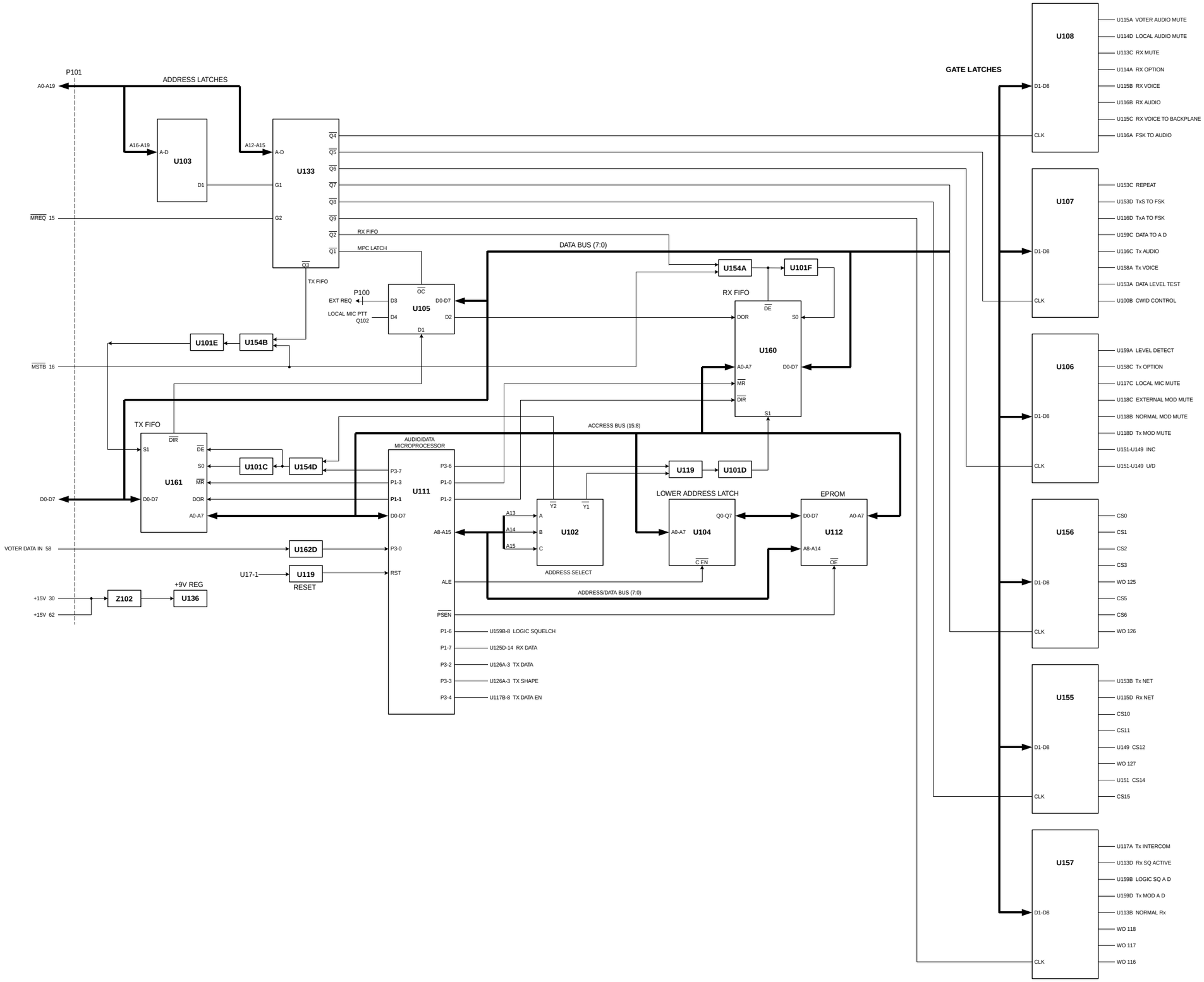
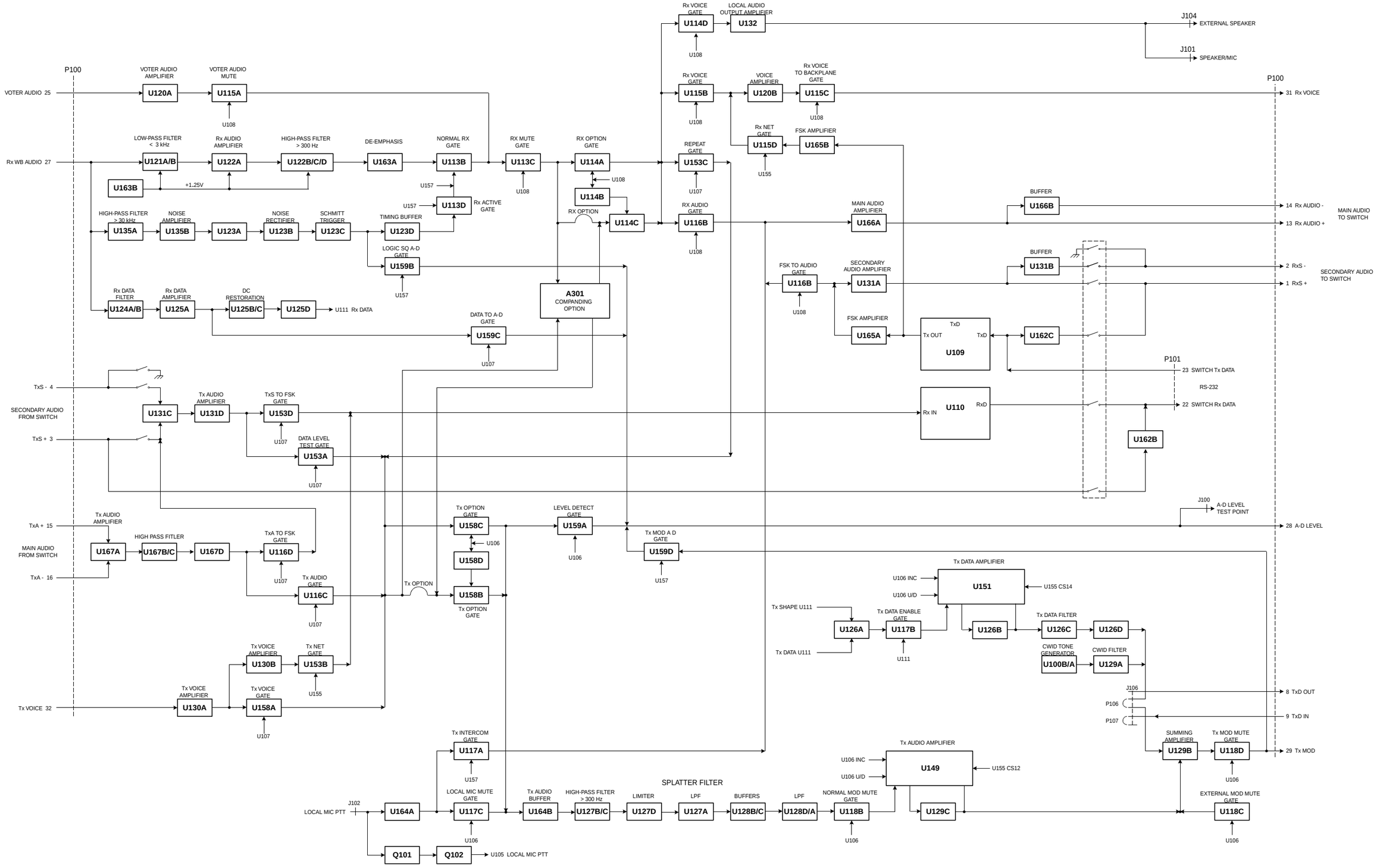
MPC BLOCK DIAGRAM
FIGURE 6-17

FOLDOUT



MAC LOGIC BLOCK DIAGRAM
FIGURE 6-18



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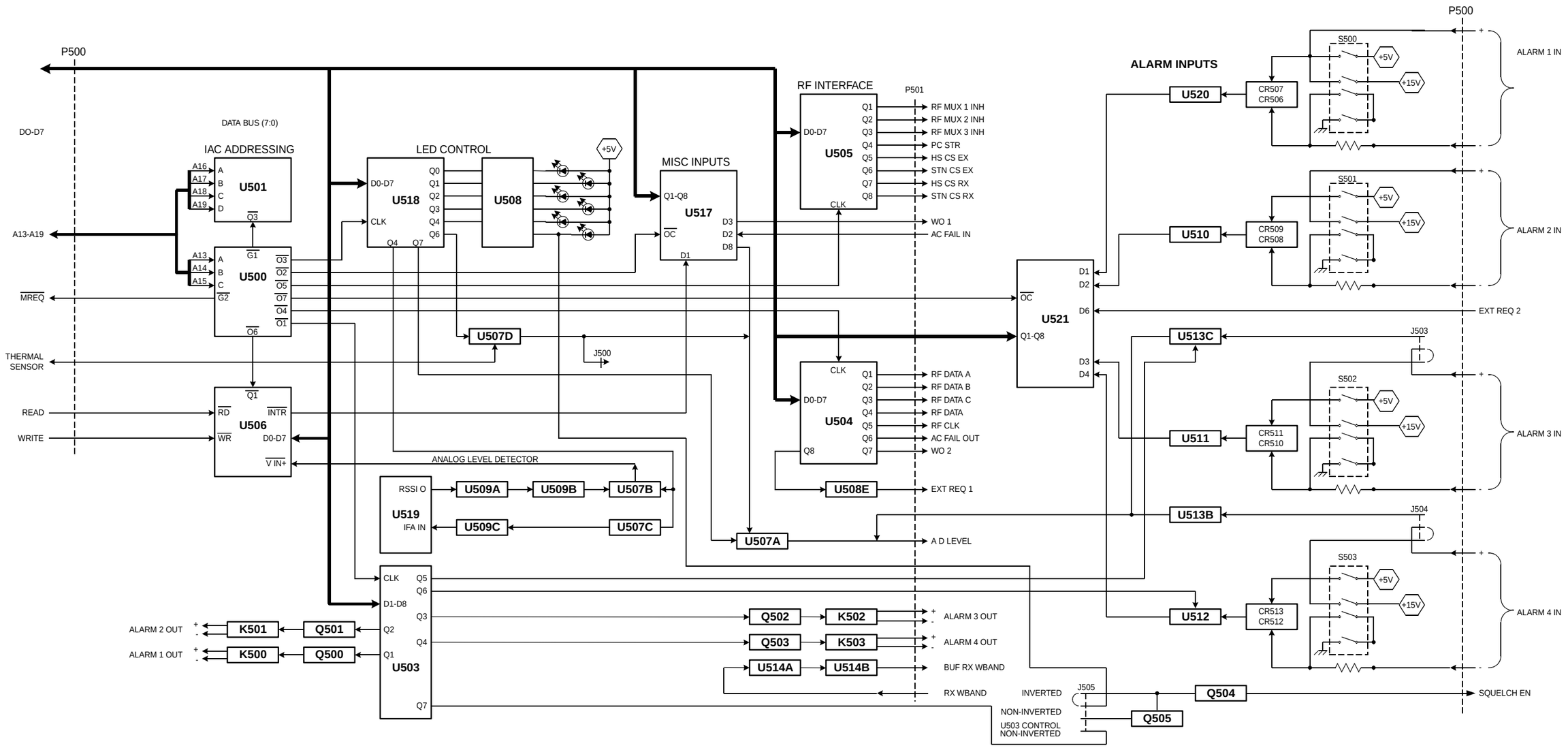
Part No. 001-2008-203

MAC AUDIO BLOCK DIAGRAM
FIGURE 6-19

FOLDOUT



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IAC BLOCK DIGARM
FIGURE 6-20
6-46