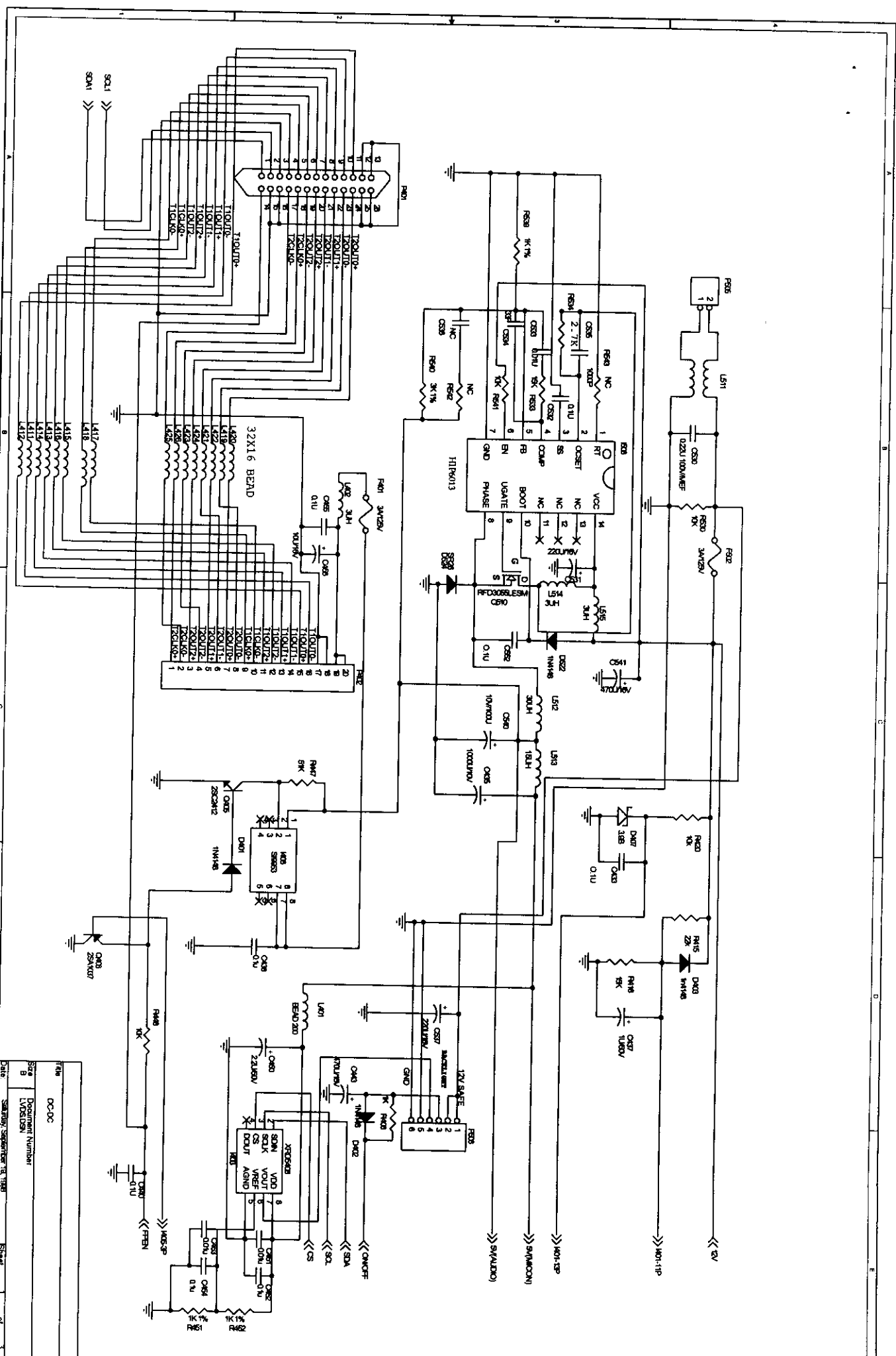
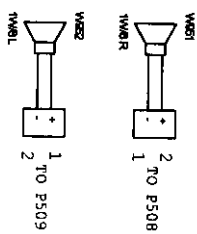
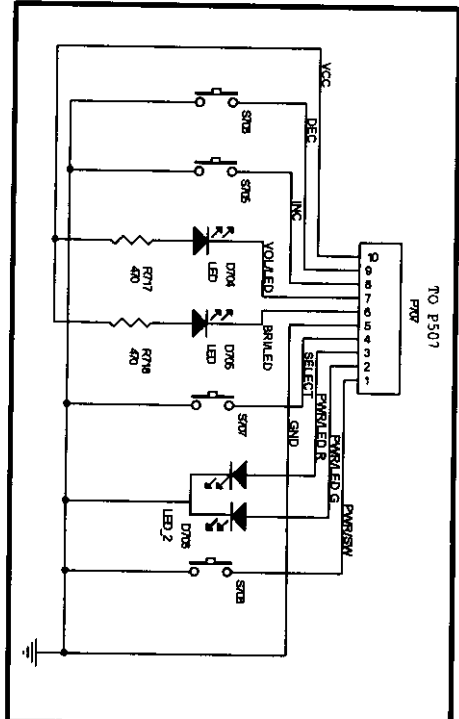
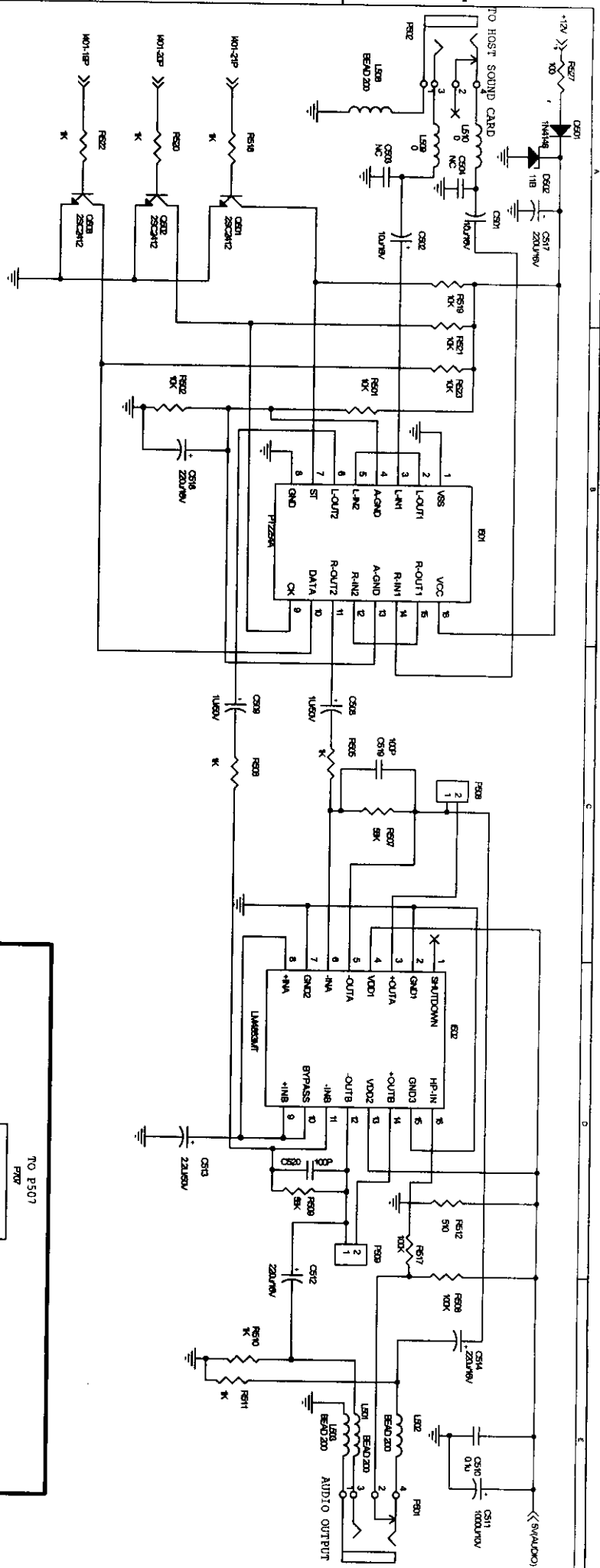


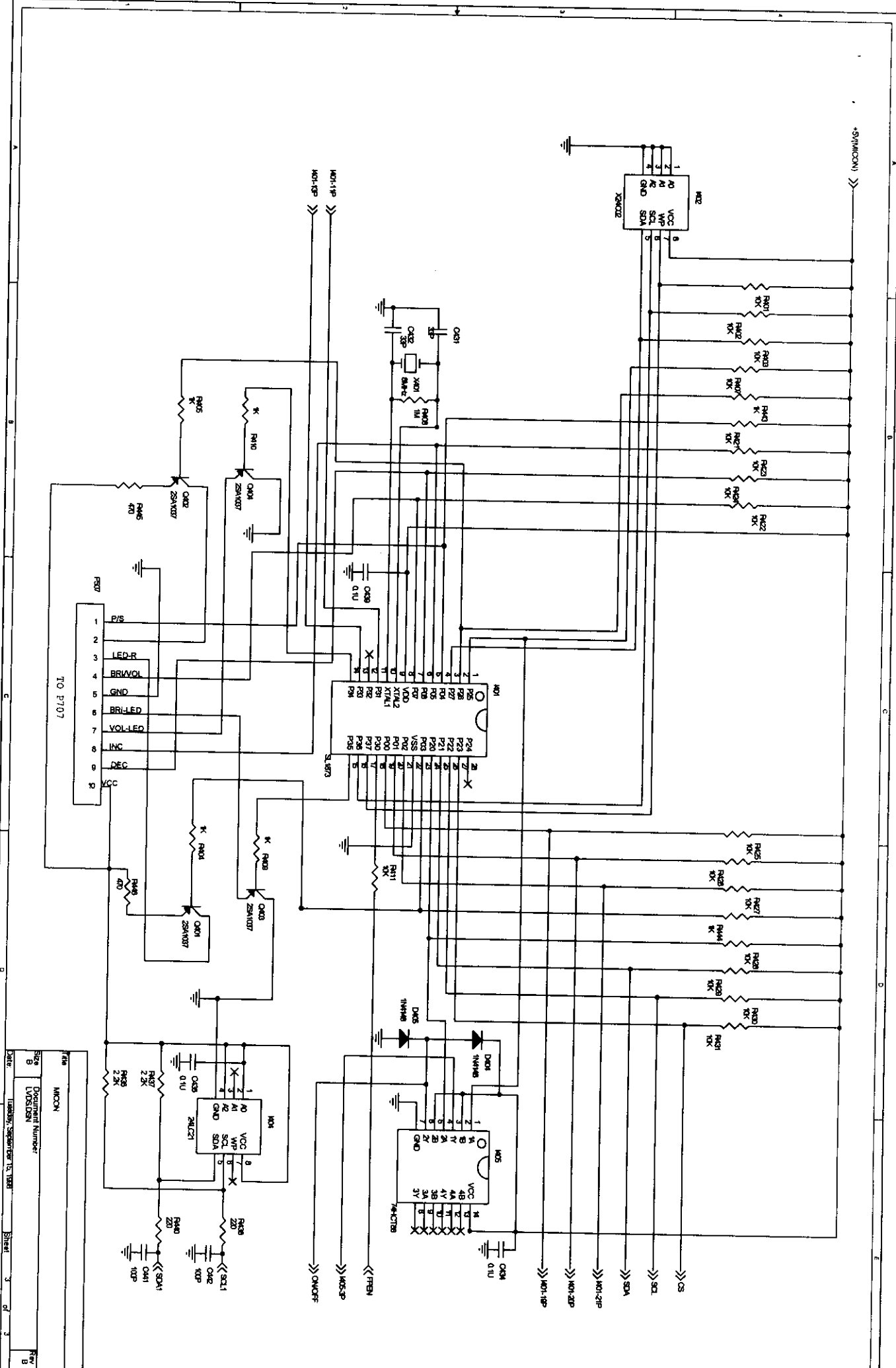
控制系統



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| File | DC-DC |
| Document Number | LVDS05N |
| Size | B |
| Date | 2005/08/14 13:58 |



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| File | ALDO |
| Size | Document Number |
| Doc | 17010101 |
| Date | SATURDAY, SEPTEMBER 11, 1988 |
| Sheet | 2 of 3 |
| Rev | B |



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|----------|--------|---------|----------|
| REV | 1 | DATE | 11/18/81 |
| DESIGNER | BRUNN | CHECKED | |
| APP'D | | DATE | 3/1/81 |
| DOC NO. | 111111 | REV | 1 |
| REV | 1 | DATE | 11/18/81 |
| DESIGNER | BRUNN | CHECKED | |
| APP'D | | DATE | 3/1/81 |
| DOC NO. | 111111 | REV | 1 |

TO P107

IC402: VCC, WP, SCL, SDA, GND

IC401: P24, P23, P22, P21, P20, P19, P18, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, P7, P6, P5, P4, P3, P2, P1, VDD, XTAL1, XTAL2, VSS, Z1, Z2, Z3, Z4, Z5, Z6, Z7, Z8, Z9, Z10, Z11, Z12, Z13, Z14, Z15, Z16, Z17, Z18, Z19, Z20, Z21, Z22, Z23, Z24, Z25, Z26, Z27, Z28, Z29, Z30, Z31, Z32, Z33, Z34, Z35, Z36, Z37, Z38, Z39, Z40, Z41, Z42, Z43, Z44, Z45, Z46, Z47, Z48, Z49, Z50, Z51, Z52, Z53, Z54, Z55, Z56, Z57, Z58, Z59, Z60, Z61, Z62, Z63, Z64, Z65, Z66, Z67, Z68, Z69, Z70, Z71, Z72, Z73, Z74, Z75, Z76, Z77, Z78, Z79, Z80, Z81, Z82, Z83, Z84, Z85, Z86, Z87, Z88, Z89, Z90, Z91, Z92, Z93, Z94, Z95, Z96, Z97, Z98, Z99, Z100

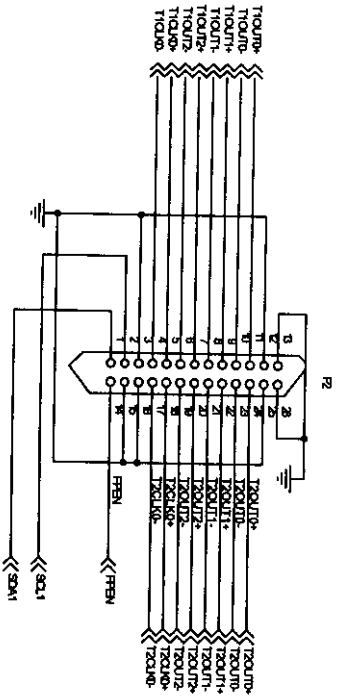
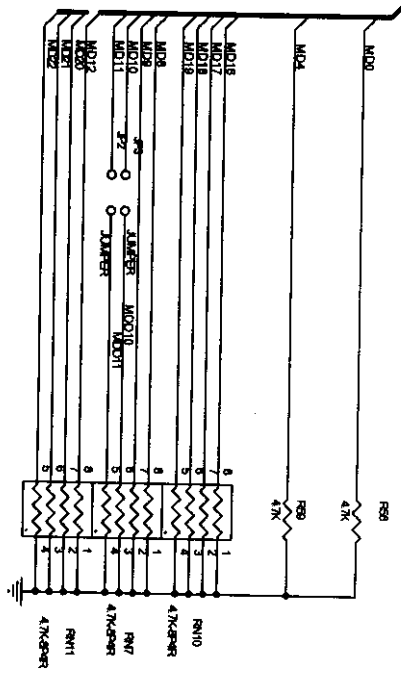
IC403: VCC, WP, SCL, SDA, GND

IC404: VCC, WP, SCL, SDA, GND

IC405: VCC, WP, SCL, SDA, GND

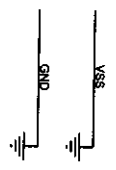
IC406: VCC, WP, SCL, SDA, GND

MD0:10



MD0 : 0=8MCLK
1=7MCLK
MD1 : 0=4MCLK
1=3MCLK Memory RAS to CAS Delay
MD2 : 0=1MB bank each
1=2MB bank each
MD3 : 0=4MCLK
1=3MCLK Memory Pre-charge time select
MD[5:4] : 10= 8-bit column address
11= 9-bit column address
0x= 10-bit column address
MD6 : 0= disable Block Write for Drawing Processor
1= Enable Block Write for Drawing Processor
MD7 : 0=EDO DRAM 1=SDRAM or SGRAM
MD8 : 0=Color TFT 1=Color STN
MD9 : 0=Normal 1=Inverted TFT FRCLK select
MD[11:10] : 00= 640x480 LCD DISPLAY SIZE
01= 800x600
10= 1024x768
11= 1280x1024

| | | |
|-----|-----|-----------|
| JP3 | JP2 | |
| ON | ON | 640X480 |
| OFF | ON | 800X600 |
| OFF | OFF | 1024X768 |
| OFF | OFF | 1280X1024 |



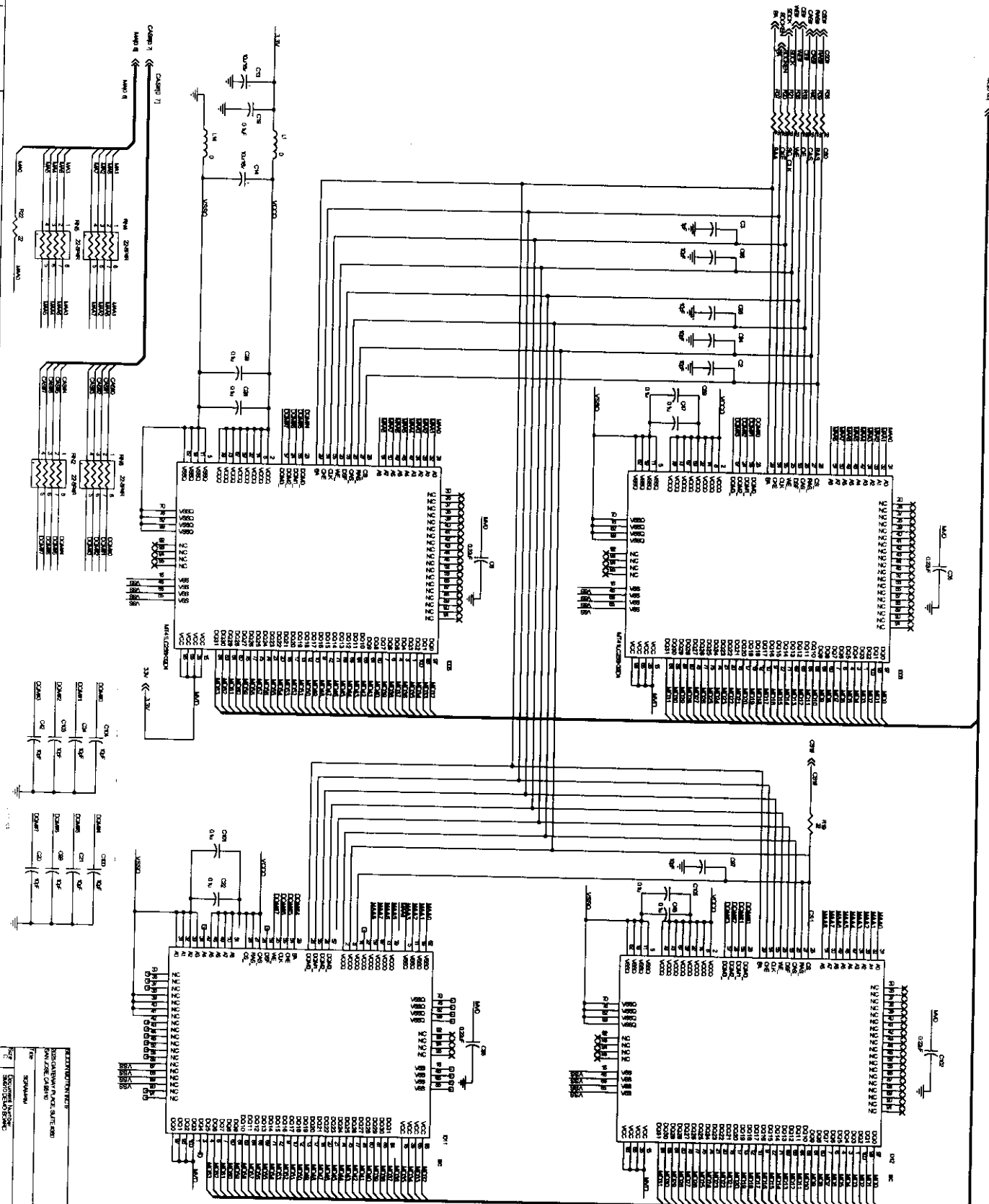
MD[14:12] : 110= 36-bit (18+18-bit , 2 pixel/clock)
100= 24-bit (12+12-bit , 2 pixel/clock)
011= 24-bit , 8-bit per R,G,B
MD15 : 0=16-bit interface DSTN Interface type
1= 24-bit interface

介面大

| | |
|-----------------|------------------------------|
| File | CONFIG & LDD PORT |
| Site | B |
| Document Number | GMASR01025N |
| Date | Thursday, September 16, 1999 |
| Sheet | 1 of 7 |
| Rev | A |

THE FIRST 2 MB

THE SECOND 2 MB



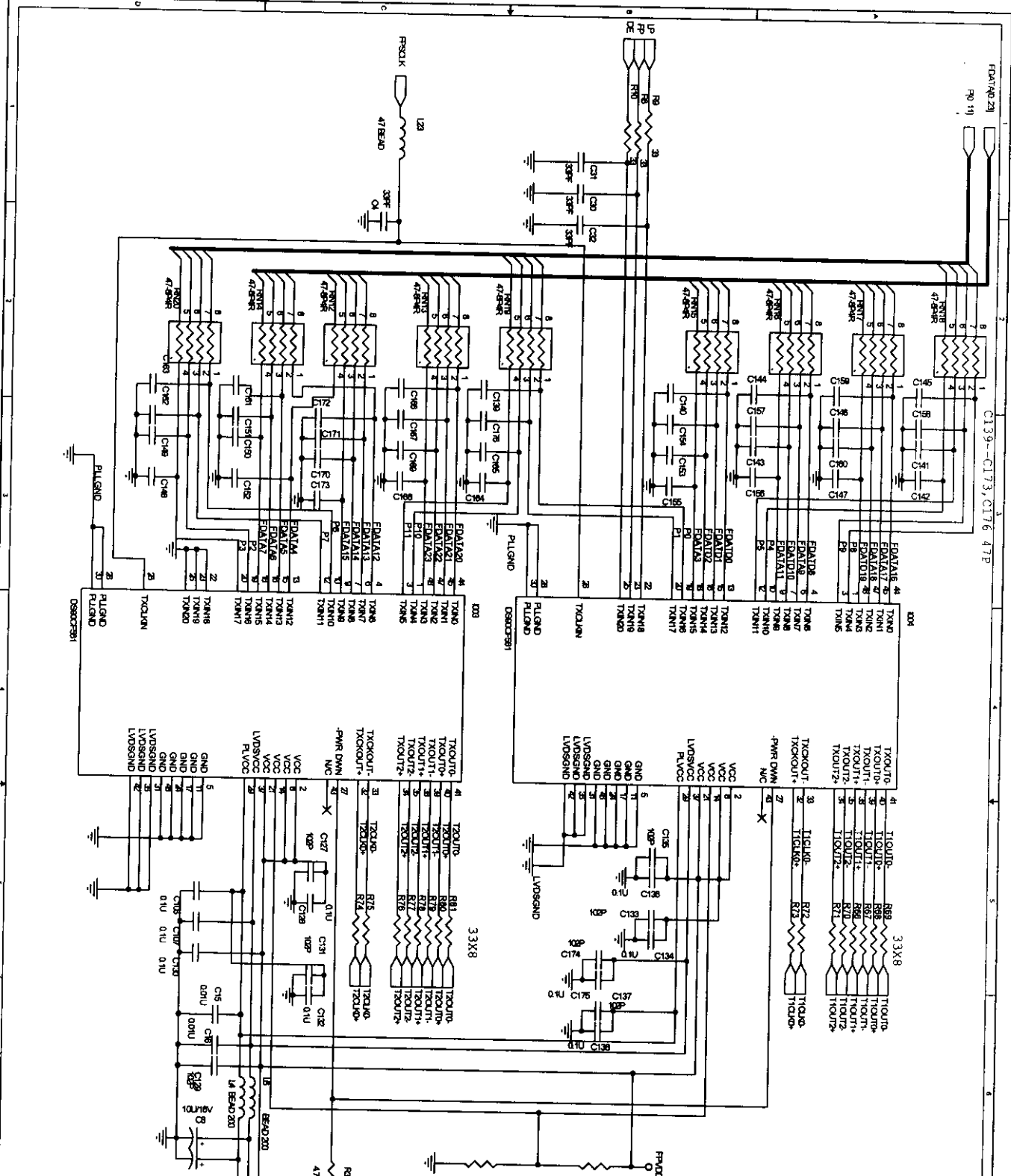
REVISIONS

| NO. | DESCRIPTION | DATE |
|-----|----------------|------|
| 1 | INITIAL DESIGN | 1978 |
| 2 | REVISION | 1978 |

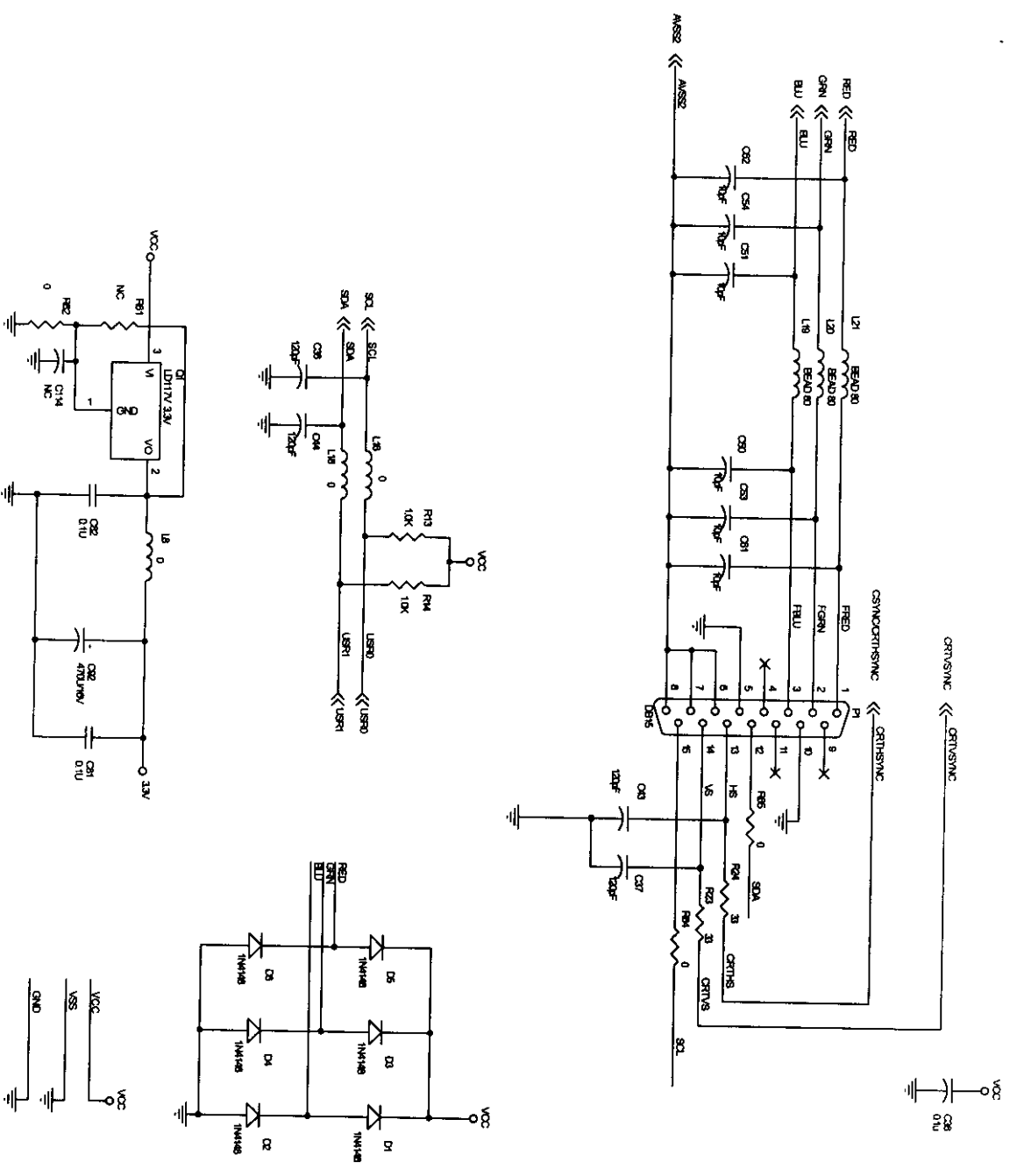
DESIGNED BY: [Name]

CHECKED BY: [Name]

DATE: [Date]



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|-------|--------------------|
| File | LVDS18 |
| Size | Document Number |
| B | 03AW58180101 |
| Date | September 13, 2001 |
| Sheet | 3 of 8 |



Saturday, September 18, 1999

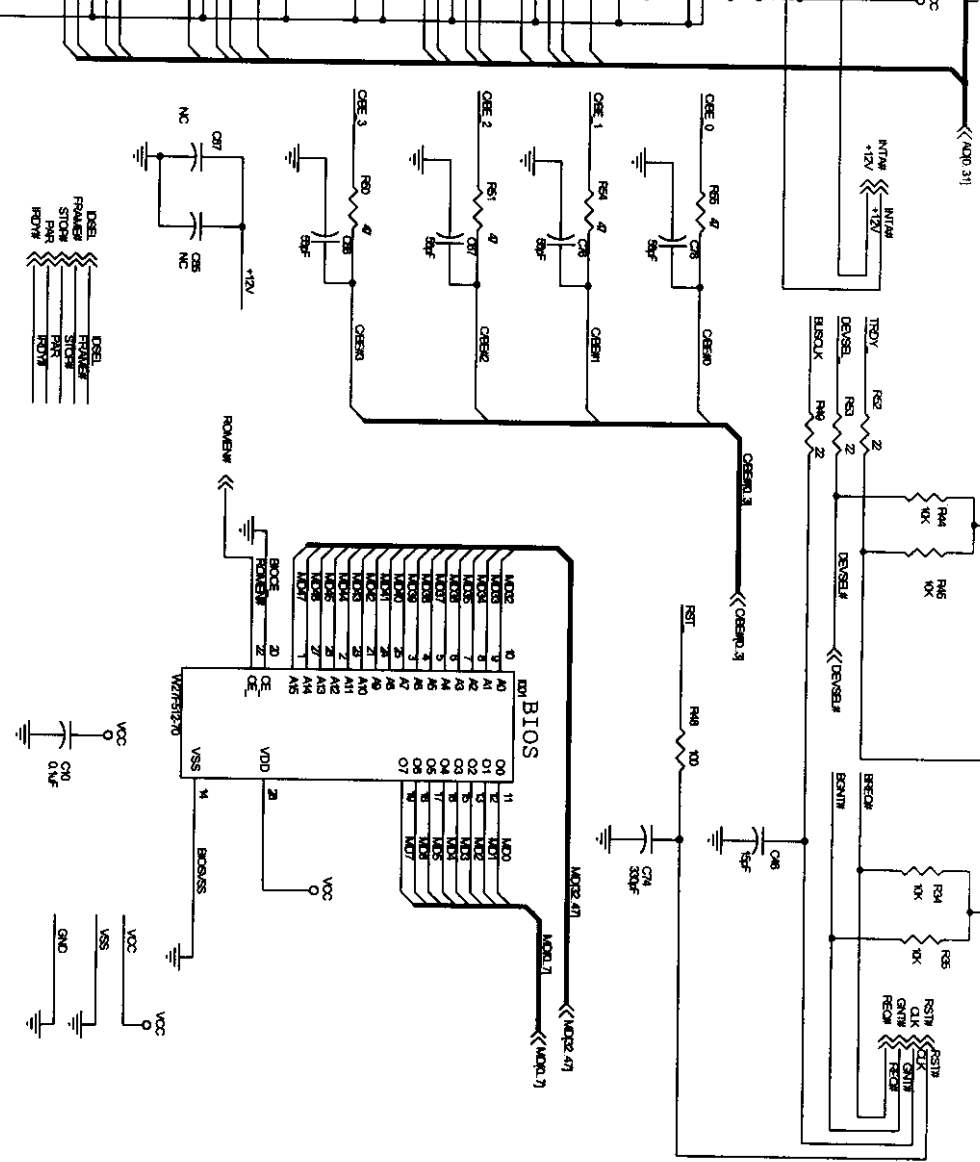
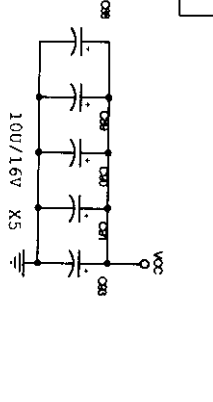
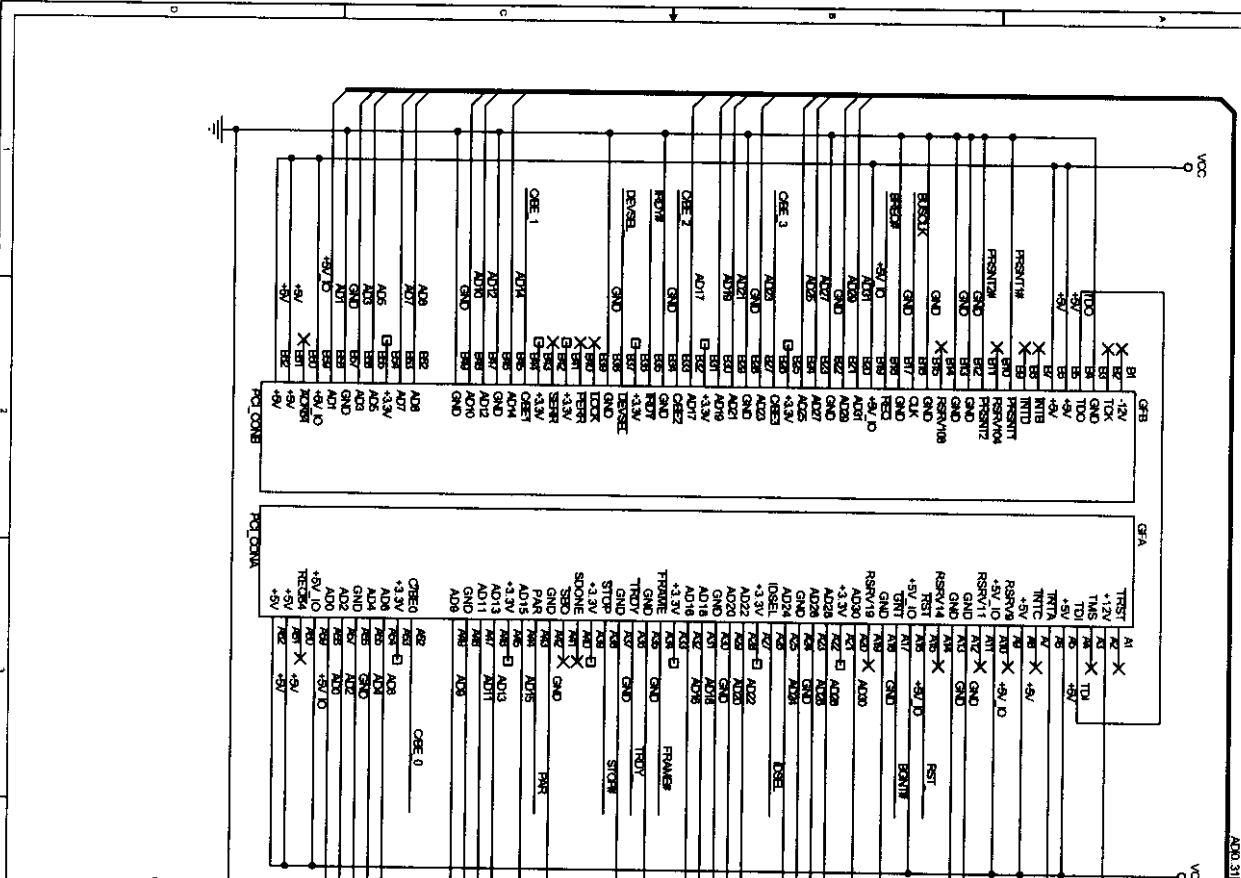
Title CRT

Size B

Document Number 0743537-001

Date Friday, September 18, 1999

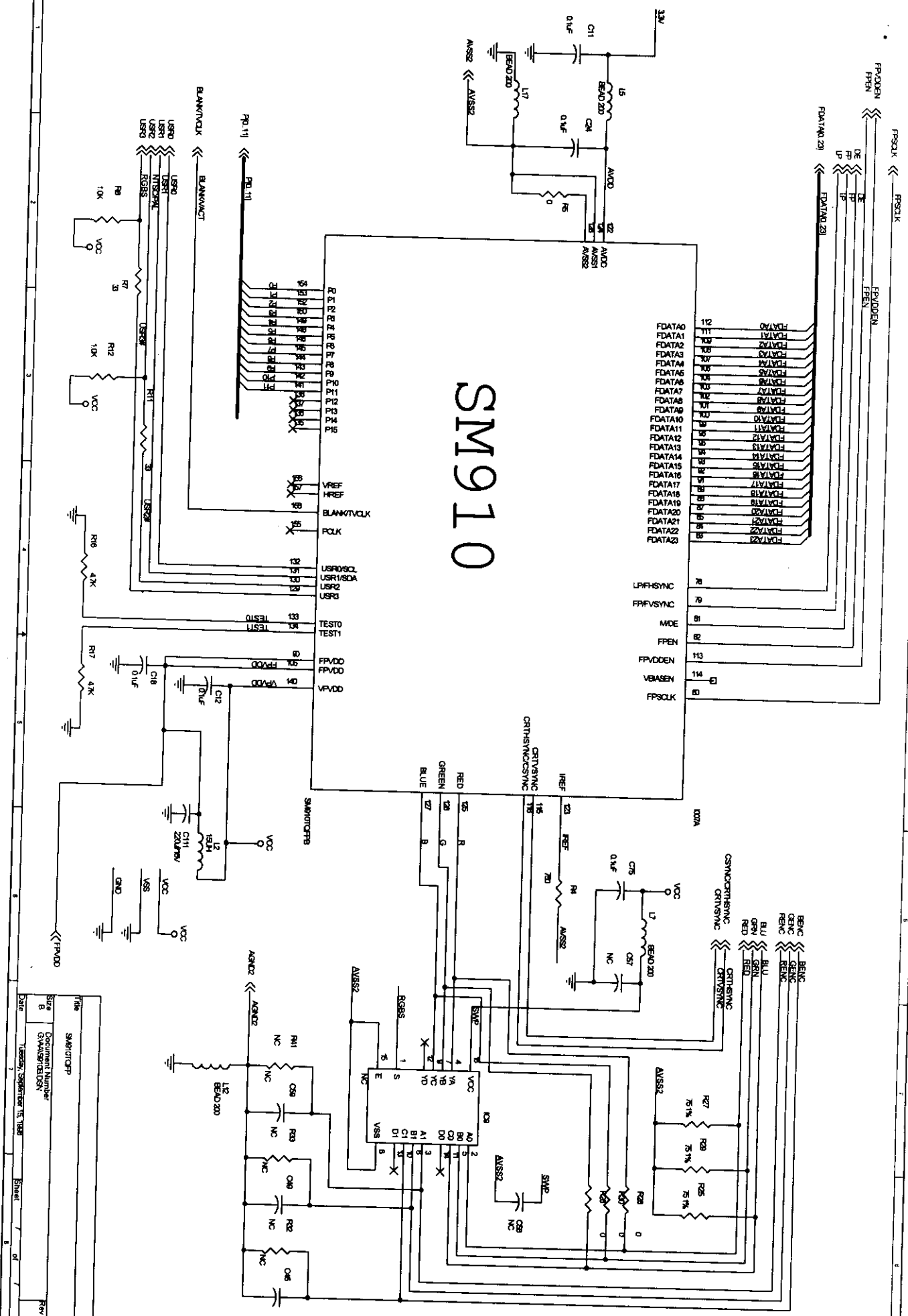
Sheet 4 of 7



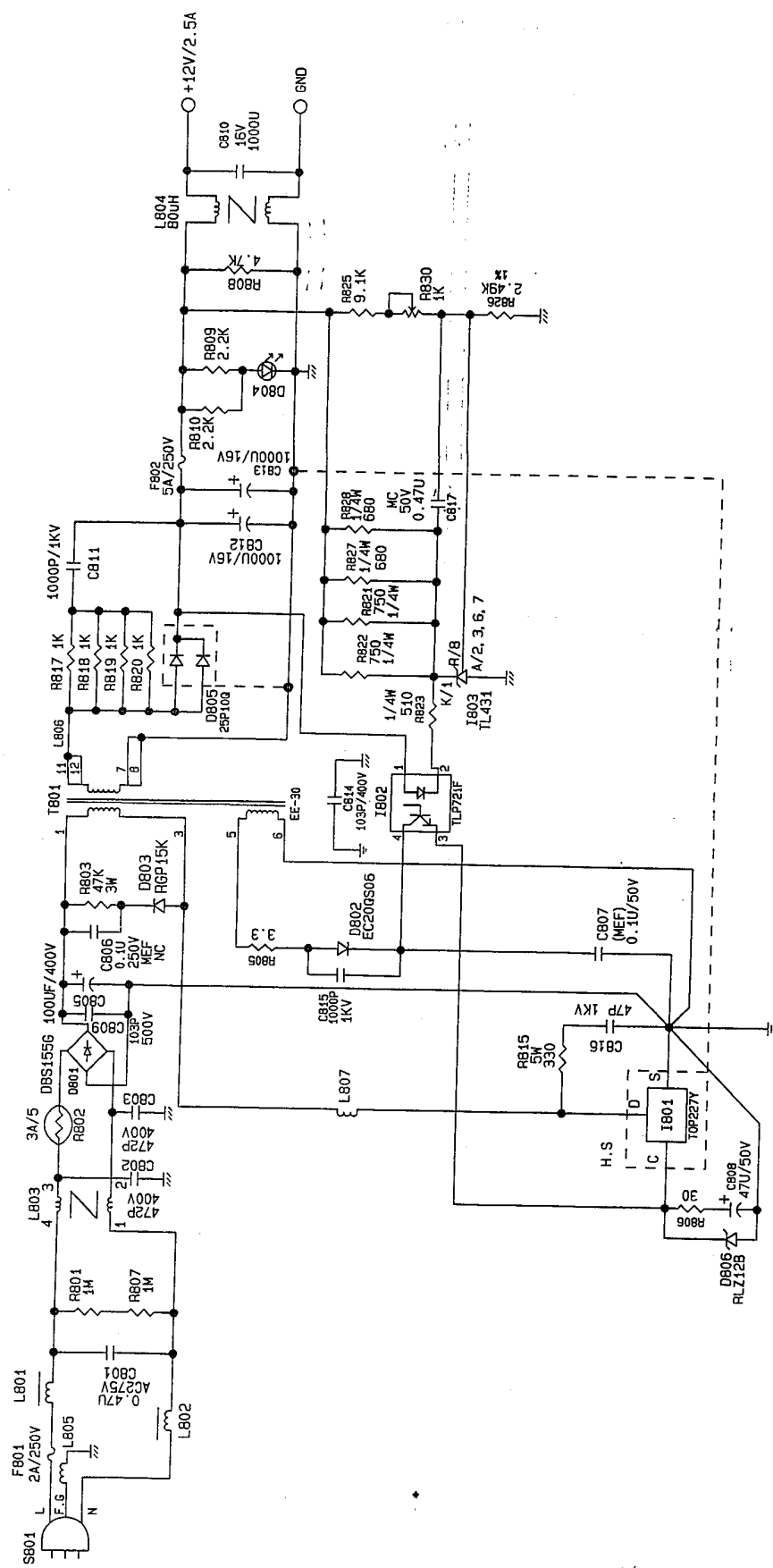
NOTE:
THIS ROW BIOS CAN BE INTEGRATED TO YOUR SYSTEM BIOS.

| | |
|-----------------|----------------|
| Title | PCI BUS & BIOS |
| Document Number | 940031 |
| Revision | B |
| Quantity | 1 |
| Date | 11/15/88 |
| Drawn by | 5 |
| Checked by | 7 |
| Approved by | 8 |

SM910



| | |
|-----------------|------------------------------|
| Title | SM910/01P |
| Size | B |
| Document Number | 0V440001005N |
| Date | Version 3 September 15, 1988 |
| Sheet | 1 of 1 |



| MARK | DATE | CONTENT | REVISION | DRAW | CHECK | APPROVAL | ISSUE |
|------|------|---------|----------|-----------------------|------------------------|----------|-----------|
| | | | | | | | 87-09-24 |
| | | | | JEAN CO., LTD | | | |
| | | | | DRAW NAME | SCHEMATIC DIAGRAM | | |
| | | | | DRAW NO | POWER BOARD (A DAPTOR) | | |
| | | | | Page: 0 | Page: 0 | NEXT: 0 | REV: 0.07 |
| | | | | I CAN MOUNTING - 3000 | | | |