Channel Frequency (Nominal) =	2440.50 MHz		
Bit Error Rate =	1.00E-04		
Required S/N for BER =	11.0 dB		
System Losses =	2.0 dB		
Desired Signal Strength at Receiver (S) =	-50.3 dBm		

Jammer Frequency (MHz)	Jammer Power (J) (dBm)	Jammer to Signal Ratio J / S (dB)	Processing Gain (dB)
2439.00	-29.80	20.5	33.5
2439.05	-31.80	18.5	31.5
2439.10	-33.13	17.2	30.2
2439.15	-34.63	15.7	28.7
2439.20	-36.15	14.2	27.2
2439.25	-37.80	12.5	25.5
2439.30	-39.80	10.5	23.5
2439.35	-41.80	8.5	21.5
2439.40	-43.63	6.7	19.7
2439.45	-45.63	4.7	17.7
2439.50	-47.30	3.0	16.0
2439.55	-48.96	1.3	14.3
2439.60	-50.30	0.0	13.0
2439.65	-51.13	-0.8	12.2
2439.70	-51.63	-1.3	11.7
2439.75	-51.80	-1.5	11.5
2439.80	-51.80	-1.5	11.5
2439.85	-51.80	-1.5	11.5
2439.90	-51.63	-1.3	11.7
2439.95	-51.63	-1.3	11.7
2440.00	-51.13	-0.8	12.2
2440.05	-51.13	-0.8	12.2
2440.10	-50.96	-0.7	12.3
2440.15	-50.80	-0.5	12.5
2440.20	-50.30	0.0	13.0
2440.25	-50.13	0.2	13.2
2440.30	-51.13	-0.8	12.2
2440.31	-51.30	-1.0	12.0
2440.33	-51.30	-1.0	12.0
2440.34	-50.13	0.2	13.2
2440.35	-49.46	0.8	13.8
2440.36	-48.63	1.7	14.7
2440.362	-48.30	2.0	15.0
2440.37	-48.80	1.5	14.5
2440.39	-50.80	-0.5	12.5
2440.40	-51.60	-1.3	11.7
2440.45	-50.63	-0.3	12.7
2440.500	-50.63	-0.3	12.7
2440.55	-50.63	-0.3	12.7
2440.60	-50.63	-0.3	12.7
2440.65	-50.96	-0.7	12.3
2440.70	-51.13	-0.8	12.2
2440.75	-51.13	-0.8	12.2
2440.80	-51.13	-0.8	12.2
2440.85	-51.63	-1.3	11.7
2440.90	-51.46	-1.2	11.8

Fchannel = 2440.5 MHz

2440.95	-51.63	-1.3	11.7
2441.00	-51.63	-1.3	11.7
2441.05	-51.46	-1.2	11.8
2441.10	-50.63	-0.3	12.7
2441.15	-49.63	0.7	13.7
2441.20	-47.96	2.3	15.3
2441.25	-46.46	3.8	16.8
2441.30	-44.30	6.0	19.0
2441.35	-42.63	7.7	20.7
2441.40	-40.80	9.5	22.5
2441.45	-39.13	11.2	24.2
2441.50	-37.46	12.8	25.8
2441.55	-35.96	14.3	27.3
2441.60	-34.46	15.8	28.8
2441.65	-33.13	17.2	30.2
2441.70	-32.13	18.2	31.2
2441.75	-31.30	19.0	32.0
2441.80	-30.30	20.0	33.0
2441.85	-29.13	21.2	34.2
2441.90	-28.46	21.8	34.8
2441.95	-27.80	22.5	35.5
2442.00	-27.13	23.2	36.2

= Minimum Processing Gain
= measured center frequency

Test Setup: Device under test = slave mode, transmitter = master mode

IC used:
LXT820B2 Tesla
FPGA basied BMC: EPF10K100ARC240-2
Code Date: 12/9/99, 11:48 am. (Meelan rev1)

Control Board:
REV 10B
Serial number: 03
MCU date code: 11/22/99

RF Board:
LXT820 DV REV 2A
serial number: 03

24.0 MHz Clock Frequency :
Device under test: 23.998646 MHz (-56.4 ppm)
Transmitter: 23.998936 MHz (-44.3 ppm)

Processing Gain Vs CW Jammer Frequency: Alpine test Fixture