======= WLAN =========

(1) Transmit Path

(a) 88W8580 (U1)

The transmitting data comes from the computer block via the 100BASE-FX conforming interface port accordig to the 100BASE-FX interface protocol. The Fast Ehternet MAC and 802.3 PHY in 88W8580(U1) perform the 100BASE-FX conforming communication control.
The incomming transmitting data is transfered to the 802.11 Dual MAC via the Internal Bus. The 802.11 Dual MAC does the protocol control, media access control, and the generation of transmit data frame.
The 802.11 Dual MAC has the carrier sense function also, then it does the carrier detection base on RSSI. The 802.11 baseband modulates the generated transmit data frame by 64QAM, 16QAM, QPSK, BPSK, CCK, DQSK, or DBPSK according to the transfer data rate, and the 802.11 baseband generates I,Q baseband signals. The DACs convert the modulated digital I,Q baseband signal to the analog baseband signals, and these analog baseband signals are delivered from 88W8580(U1) to 88W8010(U2).

(b) 88W8010 (U2)

The inputted baseband signals are converted to 482.4MHz-494.44MHz IF signal (1MHz step, 1-13 channels) according to the channel frequency by the Local Oscillator(LO) and the IF mixer.
Next, the RF Mixer converts the IF signal to the 2412MHz-2472MHz RF signal (5MHz step 1-13channels). Gain adjustment of the RF signal is carried out by the bias controlled Variable Gain Amp (VGA), it is amplified by Power Amp (PA), and 88W8010(U2) outputs the amplified RF signal.

(c) Balun(BA1), Tx/Rx SW(U6), BPF(BP1)

The Balun(BA1) converts the balanced RF signal which is provided from 88W8010(U2) to unbalanced RF signal. And it pass through the Tx/Rx SW(U6) and the Band Pass Filter BPF(BP1). The band-width of the RF signal is limitted by the BPF(BP1). The RF signal is delivered to ANT SW(U7).
The 88W8580(U1) does the timing control of the Tx/Rx SW(U6) using a control signal.

(d) ANT SW(U7)

The RF signal from BPF(BP1) is delivered to selected BGA PAD (ANT0 or ANT1) according to the 888W8580's control signal.
The ANT1 BGA PAD is connected to the Original RF Connector via the Divider. And the external monopole antenna is connected to the Original RF Connector.
Then the transmit RF signal is radiated from the monopole antenna.

(2) Receive Path

(a) ANT SW(U6)

The receiving RF signal comes from the external monopole antenna. It passes through the RF original connector and the ANT1 BGA Pad under the Wireless LAN module via the Divider and it goes into the module. The RF signal is delivered to BPF(BP1) via ANT SW(U6).

(b) BPF(BP1), Tx/Rx SW(U6), 88W8010(U2)

The receiving RF signal pass through the BPF(BP1) and its

out-of-band spurious is eliminated by the BPF. The RF signal is pass through the 88W8010(U2) via Tx/Rx SW(U6). The 88W8010(U2) amplifies the RF signal to an apropriate level RF signal by the 88W8010's Low Noise Amp(LNA).
The RF mixer generates 482.4MHz-494.4MHz IF signal (1MHz step, 1-13 channels) from the RF signal and the the 1929.6-1977.6MHz signal which is delivered from Local Oscillator(LO). The other RF mixers and filters convert from the IF signal to analog I,Q baseband signals. The analog I, Q baseband signals are amplified to an appropriate level and they are delivered to 88W8580(U1).

(c) 88W8580(U1)

The 802.11 Baseband converts the analog I, Q signals to digital baseband signals by ADCs. The digital baseband signals are demodulated to receiving data frame by 64QAM, 16QAM, QPSK, BPSK, CCK, DQSK, or DBPSK according to the transfer data rate.
The receiving data frame is provided to the 802.11 MAC and the 802.11 MAC takes the receiving data from the receiving data frame. By the receiving data is transfered to 100BASE-FX Conforming Interface via Internal Bus, 802.3PHY and Fast Ethernet MAC, the 88W8580(U1) outputs the receiving data. The computer block receives the receiving data accrding to the 100BASE-FX interface protocol.

======= Bluetooth =========

(1) Reference clock oscillator and RF frequency synthesizer block

The "Fref" reference clock is generated by IC001's oscillator circuit with X001 24MHz crystal resonator. The oscillator circuit is temperature-compensated and the tolerance of the oscillator is +/-20ppm in the temperature environment of -40 to +85 degrees C.
The "Fref" reference clock is supplied to RF synthesizer block, micro controller block and Baseband and Logic block.

The RF frequency synthesizer block has a Local Oscillator (VCO) and a RF synthesizer.
The frequency of the Local Oscillator in IC001 is 2400.5MHz to 2478.5MHz at receiving time, and 2403MHz to 2481MHz at transmitting time.

(2) RF Transmitter block

The digital baseband data is provided from the Baseband and Logic Block. 1MHz frequency offset is added to the digital baseband data. And it is converted to baseband signal by DAC.
The baseband signal is up-converted to 2.4GHz by the IQ modulator (IQ MOD). And RF amp amplifies its signal level and outputs balanced signal.

The PLL synthesizer gives local oscillator output to the IQ modulator. The synthesizer generates around 1.6GHz signal. And the synthesizer mixes 1.6GHz signal and its half frequency signal (800MHz). Then it outputs 2.4GHz signal. The 2.4GHz signal passes through the 90 digrees phase splitter, and it gives the IQ drive signal to the modulator.

The Differential signal output from the RF Amp is converted to unbalanced signal by L001,L002,L003,C009,C018.
And the unbalanced signal pass through the IC003 RF switch (Tx/Rx switch) and FL001 Tx/Rx Band Pass Filter(BPF). It passes through the IC004 RF switch (ANT switch) and deriverd to the selected output RF Pad under the Bluetooth module.

The output RF pad is connected to the Original RF original

connector, and the external monopole antenna is connected to the Original RF connector. Then the transmit signal is radiated from the monopole antenna.

(3) RF Receiving block

The receiving signal (2402 to 2480MHz) comes from the external monopole antenna. It passes through the RF original connector and the RF Pad under the Bluetooth module and goes into the Bluetooth module.
It also pass through the IC004 RF Switch (ANT SW)and the FL001 Tx/Rx BPF, and its out-of-band spurious is eliminated by the BPF. Next, it pass through the IC003 RF switch (Tx/Rx switch), it is amplified by IC006 Low Noise Amp(LNA) and it is provided to the internal LNA in the IC001.

The receiving signal is amplified by the internal LNA and it passes the IQ demodulator (IQ DEMOD) and the BPF. The IQ demodulator and the BPF converts the receiving signal to 1st IF signal(1.5MHz). The local oscillator signal, which is used at the IQ demodulator, is generated by the same PLL synthesizer which is used by the RF transmitting block.

The 1st IF signal, which is delivered from the BPF, is amplified and filtered by limitter amp. The 2nd orthogonal mixer converts 1st IF signal to 2nd IF signal (2.5MHz). The 2nd IF signal is amplified and filtered and it becomes the digital signal.
Then it passes through the demodulator and the signal delivered to Baseband and Logic block.

(3) Microcontroller block

The Microcontroller is included in IC001. And it controlles the whole hardware system with IC002 Flash Memory.
The Microcontroller fetches the program code("firmware") from the IC002 Flash Memory at power-on. And it initializes Baseband Controller and RF synthesizer, and it starts execution which is defined as the Bluetooth baseband and link manager layer.

(4) Baseband and Logic block

The functions of Bluetooth baseband and link manager layer is implemented in the IC001's Baseband and Logic block. And the Baseband and Logic block also contains the following feature.

1. To control internal PLL for the channel selection
2. To control internal RF Receiver and RF Transmitter
3. Reference signal input port
4. Port to control IC002 external memory
5. Programmable I/O ports
6. PCM data output (Audio PCM interface)
7. UART
8. Contonuous peripheral interface (SPI)
9. RAM

NOTE: Please refer the following information related to FCC requirements.

Additional information in accordance with requirements of FCC 15.247 and FCC Public Notice DA 00-705

1. Hopping frequency requirements
The number of hopping frequencies is measured in accordance with FCC Public Notice DA 00-705 and reported the compliance in the test report.
On pseudorandom frequency hopping sequence the following is an example of a 79 hopping

sequence in **data transmission mode**:
47, 21, 44, 23, 42, 53, 46, 55, 33, 48, 52, 35, 50, 20, 54, 67, 56, 37, 60, 39, 58, 69, 62, 71, 64, 25, 68, 27, 66, 57, 70, 59, 72, 29, 76, 31, 74, 61, 78, 01, 63, 41, 05, 43, 03, 73, 07, 75, 09, 45, 13, 40,11, 77, 15, 00, 16, 28, 49, 22, 34, 02, 19, 06, 17, 51, 32, 14, 36, 04, 12, 26, 18, 38, 24, 08, 30, 65,10

Example of a hopping sequence in **inquiry mode** :
47, 08, 71, 57, 63, 02, 61, 45, 55, 10, 59, 73, 65, 69, 27, 43, 00, 77, 04, 67, 37, 06, 31, 75, 33, 39, 51, 40, 29, 14, 35, 49

Example of a hopping sequence in **paging mode**:
08, 57, 70, 68, 51, 02, 40, 42, 04, 61, 46, 44, 63, 14, 50, 48, 16, 65, 54, 52, 67, 18, 58, 56, 20, 53, 60, 62, 55, 06, 66, 64

■Adaptive Frequency Hopping (AFH/EDR) function
This product has the AFH function in Bluetooth specification V2.0 +EDR.
The AFH/EDR function restrains interference from other 2.4GHz products.
Hopping frequency is reduced for using AFH/EDR.