1 RECEIVER CIRCUITS

1-1 ANTENNA SWITCHING CIRCUIT

The antenna switching circuit functions as a low-pass filter while receiving and as resonator circuit while transmitting. The circuit does not allow transmit signals to enter receiver circuits.

Received signals enter the MAIN unit from the antenna connector and pass through the low-pass filter (L23–L25, C134, C136–C139). The signals are then applied to the RF circuit via the antenna switching circuit (D17, L26, L27, C141–C143).

1-2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through a tunable bandpass filter (D1, L1. C2–C4) where the object signals are led to the RF amplifier circuit (Q2).

The amplified signals at Q2 are applied to the 3-stage tunable bandpass filter (D2–D4, L2–L4, C13, C14, C16–C18, C20–C24) to suppress unwanted signals and improve the selectivity. The signals are then applied to the 1st mixer circuit.

D1–D4 employ varactor diodes, that are controlled by the PLL lock voltage, to track the band pass filters.

1-3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a 1st LO (VCO output) frequency. By changing the 1st LO frequency, only the desired frequency will pass through a pair of crystal filters at the next stage of the mixer.

The signals from the RF circuit are mixed with the VCO signals at the 1st mixer circuit (Q3) to produce a 21.7 MHz 1st IF signal.

The 1st IF signal is applied to a pair of crystal filters (FI1, FI2) to suppress out-of-band signals and is then amplified at the IF amplifier (Q4). The amplified signal is applied to the 2nd mixer circuit (IC1).

1-4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

The FM IF IC (IC1) contains the 2nd local oscillator, 2nd mixer, limiter amplifier, quadrature detector, and noise detector circuits, etc.

The 1st IF signal from Q4 is applied to the 2nd mixer section of IC1 (pin 16), and is mixed with a 21.25 MHz 2nd LO signal generated at the PLL circuit using the reference frequency (21.25 MHz) to produce a 450 kHz 2nd IF signal.

The 2nd IF signal from IC1 (pin 3) is passed through the ceramic filter (FI3), where unwanted signals are suppressed, and is then applied to the 2nd IF (limiter) amplifier in IC1 (pin 5). The signal is applied to the FM detector section in IC1 for demodulation into AF signals.

The FM detector circuit employs a quadrature detection method (linear phase detection), which uses a ceramic discriminator (X1) for phase delay to obtain a non-adjusting circuit. The detected signal from IC1 (pin 9) is applied to the AF circuit.

1-5 AF AMPLIFIER CIRCUIT

The AF amplifier circuit amplifies the detected signals to drive a speaker. The AF circuit includes an AF mute circuit for the squelch.

AF signals from IC1 (pin 9) are applied to the de-emphasis circuit (R118, C182). The de-emphasis circuit is an integrated circuit with frequency characteristic of –6 dB/octave.

The integrated signals are applied to the active filters (Q24, Q25) via the analog switch (IC12, pins 10, 11). Q24 functions as a high-pass filter to suppress unwanted lower noise signals and Q25 functions as a low-pass filter to suppress higher noise signals.

The filtered signals are passed through the [VOLUME] control, and are then applied to the AF power amplifier (IC14, pin 1). The output signal from IC14 (pin 4) drives the internal (external) speaker.

1-6 SQUELCH CIRCUIT

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

A portion of the AF signals from the FM IF IC (IC1, pin 9) pass through the [SQUELCH] control pot (R33), and are then applied to the active filter section (IC1, pin 8). The active filter section amplifies and filters noise components. The filtered signals are applied to the noise detector section and output from pin 14 as the “SQLI” signal. The “SQLI” signal is amplified at the DC amplifier (IC20) and applied to the CPU (IC16, pin 39) as the “SQL” signal. The CPU analyzes the noise condition and outputs the “RMUTM”, “RMUTS” signals to toggle the AF mute switches (Q26, Q27).

2 TRANSMITTER CIRCUITS

2-1 MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies audio signals with +6 dB/octave pre-emphasis from the microphone to a level needed at the modulation circuit.

The AF signals from the microphone are amplified at the microphone amplifier (IC11a) via the analog switch (IC10, pins 11, 10). A capacitor (C214) and resistor (R147) are connected to the amplifier to obtain the pre-emphasis characteristics.

The amplified signals are applied to the IDC amplifier (IC13a, pin 2) via the analog switch (IC12, pins 8, 9 and pins 4, 3) and are passed through the splatter filter (IC13b) to suppress unwanted 3 kHz or higher signals. The filtered signals are then applied to the modulation circuit.

2-2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

Audio signals from the splatter filter (IC13b) pass through the frequency deviation adjustment pot (R172) and are then applied to the modulation circuit (D8) to change the reactance of D8, and modulate the oscillated signal at the TX-VCO (Q7).

2-3 DRIVE AMPLIFIER CIRCUIT

The drive amplifier circuit amplifies the VCO oscillating signal to a level needed at the power amplifier.

The VCO output is buffer-amplified by Q9 and Q10, and is then applied to the Tx/Rx switch (D12). The transmit signal from the Tx/Rx switch is amplified to the pre-drive (Q11) and drive (Q12) amplifiers to obtain an approximate 200 mW signal level. The amplified signal is then applied to the RF power amplifier (IC3).

2-4 POWER AMPLIFIER CIRCUIT

The power amplifier circuit amplifies the driver signal to an output power level.

IC3 is a power module which has amplification output capabilities of about 35 W with 300 mW input. The output from IC3 (pin 4) is passed through the antenna switching circuit (D16) and is then applied to the antenna connector via the low-pass filter.

2-5 APC CIRCUIT

The APC circuit stabilizes transmit output power.

The RF output signal from the power amplifier (IC3) is detected at the power detector circuit (D14, D15, L21) and is then applied to one of the differential amplifier inputs (Q16, pin 5) via the High/Low control circuit (R84, Q17). The applied voltage controls the differential amplifier output (Q16, pin 2) and the bias voltage control (Q14). Thus the APC circuit maintains a constant output power.

3 PLL CIRCUITS

3-1 GENERAL

The PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL circuit compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by a crystal oscillator and the divided ratio of the programmable divider.

IC2 is a dual PLL IC which controls both VCO circuits for Tx and Rx, and contains a prescaler, programmable counter, programmable divider phase detector, charge pomp and etc.

The PLL circuit, using a one chip PLL IC (IC2), directly generates the transmit frequency and receive 1st IF frequency with VCOs. The PLL sets the divided ratio based on serial data from the CPU and compares the phases of VCO signals with the reference oscillator frequency. The PLL IC detects the out-of-step phase and output from pins 8 and 13 for Tx and Rx, respectively. The reference frequency (21.25 MHz) is oscillated at X2.

3-2 TX LOOP

The generated signal at the TX-VCO (Q7, D6–D8) enters the PLL IC (IC2, pin 2) and is divided at the programmable divider section and is then applied to the phase detector section.

The phase detector compares the input signal with a reference frequency, and then outputs the out-of-phase signal (pulse-type signal) from pin 8.

The pulse-type signal is converted into DC voltage (lock voltage) at the loop filter (R252–R254, C292–C294), and then applied to varactor diodes (D6, D7) of the TX-VCO to stabilize the oscillated frequency.

3-3 RX LOOP

The generated signal at the RX-VCO (Q8, D9, D10) enters the PLL IC (IC2, pin 19) and is divided at the programmable divider section and is then applied to the phase detector section.

The phase detector compares the input signal with a reference frequency, and then outputs the out-of-phase signal (pulse-type signal) from pin 13.

The pulse-type signal is converted into DC voltage (lock voltage) at the loop filter (R255–R257, C295, C296), and then applied to varactor diodes (D9, D10) of the RX-VCO to stabilize the oscillated frequency. The lock voltage is also used for the receiver circuit for the bandpass filter center frequency. The lock voltage from the loop filter is amplified at the buffer-amplifier (Q6) and then applied to the RF circuit.

3-4 VCO CIRCUIT

The VCO outputs from Q7 (Tx) and Q8 (Rx) are buffer-amplified at Q9 and Q10, and are then sent to the Tx/Rx switch (D11, D12). The receiver LO signal is applied to the 1st mixer circuit (Q3) through a low-pass filter, and the transmitter signal is applied to the pre-drive amplifier (Q11). A portion of the VCO output is reapplied to the PLL IC (IC2, pin 2 or pin 13) via Q5.

3-5 DSC ENCODE CIRCUIT

The DSC signal created at CPU (IC16) is passed through the buffer amplifier (Q33) and applied to the analog switch (IC12). The analog switch (IC12) is a modulation switch that switches between microphone audio signal and DSC signal.

3-6 DSC DECODE CIRCUIT

The AF signals from FM IF IC (IC1, pin 9) are filtered at the bandpass filter (IC4) with +18 dB/octave characteristics. IC4b functions as a low-pass filter to suppress unwanted higher noise signals and IC4a functions as a high-pass filter to suppress lower noise signals. The filtered signals are converted analog signals into digital signals at DSC decoder IC (IC5), and are then applied to the CPU (IC16) after shaping waveform at IC6.

4 POWER SUPPLY CIRCUITS

HV: The voltage from the connected DC power supply.
HVS: Same voltage as the HV line which is passed through the [PWR] switch (LOGIC unit; S1).
HVS: Same voltage as the HVS line which is passed through the power controller (RL1).
8V: Common 8 V converted from the VCC line at the 8V regulator circuit (IC8).
A5V: Common 5 V converted from the 8V line at the analog 5V regulator circuit (IC9).
D5V: Common 5 V converted from the 8V line at the digital 5V regulator circuit (IC7).
T8V: Transmit 8 V controlled by the T8 control circuit (Q20, Q21) using the SEND signal from CPU.
R8V: Receive 8 V controlled by the R8 control circuit (Q22, Q23) using the RCV signal from CPU. The controlled voltage is applied to the receiver circuits.

5 LOGIC CIRCUITS

5-1 MAIN UNIT

• MPU

IC16 is 16 bit multifunction microcomputer and contains FLASH memory, serial I/O, timer, A/D converter, D/A converter, programmable I/O, ROM and RAM.

• SYSTEM CLOCK CIRCUIT (MAIN UNIT)

X3, X4 are crystal oscillators and oscillated 7.9872 MHz and 32.768 kHz system clocks for the MPU (IC16) respectively.

• RESET CIRCUIT (MAIN UNIT)

IC15 is a reset IC. When turn power ON, IC15 outputs a reset signal (“LOW” pulse) to MPU (IC16, pin 75).

• LOW BATTERY DETECTOR (MAIN UNIT)

VCC voltage is divided by R204, R205 and is applied to the low battery detector circuit in the MPU (IC16, pin 42).

5-2 LOGIC UNIT

• CPU

IC1 is 8 bit single chip microcomputer and contains LCD driver, serial I/O, timer, A/D converter, programmable I/O, ROM and RAM.

• SYSTEM CLOCK CIRCUIT

X1 is a ceramic oscillator and oscillated a 4.91 MHz system clock for the CPU (IC1).

• LCD DRIVER

IC2 is a LCD driver for a dot matrix LCD.

• DIMMER CIRCUIT

CPU (IC1) and Q2, Q3, Q8 are dimmer circuit and control the LCD backlight (LED).

• CONTRAST CIRCUIT
CPU (IC1) and Q1, Q4 are contrast circuit and control the 8 step display contrast.