WCX040-FC
Hardware Design

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1 Introduction

This document defines the WCX040-FC and describes its air interface and hardware interfaces which are connected with your applications. With this document, you can quickly understand module interface specifications, RF performance, electrical and mechanical details, as well as other related information of the module.

1.1. Text Conventions

Table 1: Text Conventions

NOTE	"**NOTE**" is used to identify important information. When you see "**NOTE**" in this document, please be aware that the information contained therein may be crucial for understanding, implementing, or operating related technologies or steps. We strongly recommend that you pay special attention to these "**NOTE**" sections while reading the document to ensure that you can use this technical documentation correctly and efficiently.
[…]	Brackets ([…]) enclosing a range of numbers after a pin name indicate all pins of the same type within that range. For instance, SDIO_DATA[0:3] denotes all four SDIO pins, namely: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

WCX040-FC is a long-range and low-power Wi-Fi HaLow module compliant with IEEE 802.11ah Wi-Fi standard. It operates in Sub-1 GHz frequency band, features 32.5 Mbps maximum transmission rate and provides an SDIO 2.0 interface for Wi-Fi application.

It is an SMD module with compact packaging. Related information is listed in the table below:

Table 2: Basic Information

WCX040-FC	
Packaging type	LGA
Pin counts	40
Dimensions	(13.0 ±0.2) mm × (13.0 ±0.2) mm × (2.2 ±0.2) mm
Weight	Approx. 0.72 g

2.1. Key Features

Table 3: Key Features

Basic Information	
Protocol and Standards	● Wi-Fi protocol: IEEE 802.11ah ● All hardware components are fully compliant with EU RoHS directive
Power Supplies	**VBAT Power Supply:** ● 3.0–3.6 V ● Typ.: 3.3 V **VDD_FEM Power Supply:** ● 3.0–3.6 V ● Typ.: 3.3 V **VDD_IO Power Supply [1]:** ● 1.8–3.6 V ● Typ.: 3.3 V
Temperature Ranges	● Operating temperature [2]: -30 to +85 °C ● Extended temperature: -40 to +85 °C ● Storage temperature: -40 to +95 °C
EVB Kit	WCX040-FC-M.2, RK3568-WF EVB [3]

[1] The VDD_IO power supply should not exceed VBAT.
[2] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes and vapor chambers. Within this range, the module's indicators comply with IEEE requirements.
[3] For more details about the EVB, see ***document [1]***.

RF Antenna Interface	
Antenna Interface	● ANT_WIFI ● 50 Ω characteristic impedance
Application Interface	
Application Interfaces	SDIO 2.0, JTAG

3 RF Performances

3.1. Wi-Fi Performances

Table 4: Wi-Fi Performances

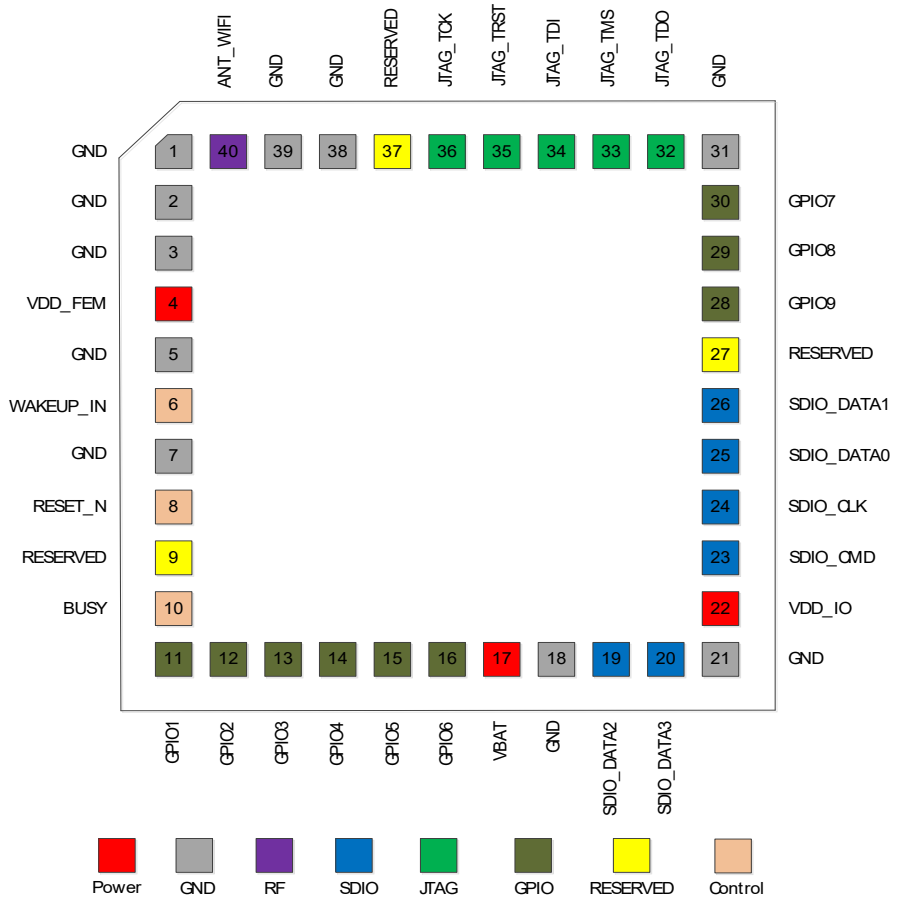
Operating Frequency				
Sub-1 GHz: 902–928 MHz				
Modulation				
OFDM, BPSK, QPSK, 16QAM, 64QAM				
Operating Mode				
● AP ● STA				
Encryption Mode				
AES, SHA-256, SHA-384, SHA-512, WPA3, OWE				
Transmission Data Rate				
● 1 MHz: MCS 0–MCS 7, MCS 10 ● 2 MHz: MCS 0–MCS 7 ● 4 MHz: MCS 0–MCS 7 ● 8 MHz: MCS 0–MCS 7				
Condition (VBAT = 3.3 V, VDD_FEM = 3.3 V, VDD_IO = 1.8 V; Temp. = 25 °C)		**EVM**	**Typ.; Unit: dBm; Tolerance: ±2 dB**	
			Transmitting Power	**Receiver Sensitivity**
Sub-1 GHz	802.11ah, 1 MHz @ MCS 0	≤ -5 dB	21	-108
	802.11ah, 2 MHz @ MCS 0		20	-104
	802.11ah, 4 MHz @ MCS 0	≤ -5 dB	20	-102
	802.11ah, 8 MHz @ MCS 0	≤ -5 dB	20	-98

802.11ah, 1 MHz @ MCS 7	≤ -27 dB	17	-88
802.11ah, 2 MHz @ MCS 7	≤ -27 dB	17	-84
802.11ah, 4 MHz @ MCS 7	≤ -27 dB	17	-82
802.11ah, 8 MHz @ MCS 7	≤ -27 dB	17	-77
802.11ah, 1 MHz @ MCS 10	≤ -5 dB	21	-109

4 Application Interfaces

4.1. Pin Assignment

Figure 1: Pin Assignment (Top View)



NOTE

1. Keep all RESERVED pins unconnected.
2. All GND pins should be connected to ground.
3. Keep all unused GPIO pins (GPIO1–GPIO9) pulled down to GND via 10 kΩ resistors.
4. All unused digital I/O pins must be pulled up or down to ensure they are connected, otherwise more leakage current in VDD_IO power supply will be generated.

4.2. Pin Description

Table 5: Parameter Definition

Parameter	Description

AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply and GND Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	17	PI	Power supply for the module	Vmax = 3.6 V Vmin = 3.0 V Vnom = 3.3 V	It must be provided with sufficient current of at least 0.5 A.
VDD_FEM	4	PI	Power supply for the FEM	Vmax = 3.6 V Vmin = 3.0 V Vnom = 3.3 V	
VDD_IO	22	PI	Power supply for the I/O pins	Vmax = 3.6 V Vmin = 1.8 V Vnom = 3.3 V	
GND	1–3, 5, 7, 18, 21, 31, 38, 39				
Wi-Fi Application Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDIO_CLK	24	DI	SDIO clock	VDD_IO	SDIO 2.0 compliant. **SDIO mode**: Require differential impedance of 50 Ω. Reserve 10–100 kΩ resistors to pull each of them up to VDD_IO. **SPI mode (Slave mode only):** Switch to SPI mode by controlling SDIO_DATA3 and SDIO_CMD. For details, please consult NetPrisma Technical Support.
			SPI clock		
SDIO_CMD	23	DIO	SDIO command		
		DI	SPI master-out slave-in		
SDIO_DATA0	25	DIO	SDIO data bit 0		
		DO	SPI master-in slave-out		
SDIO_DATA1	26	DIO	SDIO data bit 1		
		DI	SPI interrupt		
SDIO_DATA3	20	DIO	SDIO data bit 3		
		DI	SPI chip select		
SDIO_DATA2	19	DIO	SDIO data bit 2		

			-		Pulled up to VDD_IO via a 47 kΩ resistor in SPI mode.

JTAG Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
JTAG_TDO	32	DO	JTAG test data out	VDD_IO	Externally pulled down to GND with 10 kΩ resistors.
JTAG_TMS	33	DI	JTAG test mode select		
JTAG_TDI	34	DI	JTAG test data in		
JTAG_TCK	36	DI	JTAG test clock		
JTAG_TRST	35	DI	JTAG test reset		Pulled down to GND with a 10 kΩ resistor inside the module.

GPIO Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GPIO1	11	DIO	General-purpose input/output	VDD_IO	If unused, pull them down to GND with 10 kΩ resistors.
GPIO2	12	DIO	General-purpose input/output		
GPIO3	13	DIO	General-purpose input/output		
GPIO4	14	DIO	General-purpose input/output		
GPIO5	15	DIO	General-purpose input/output		
GPIO6	16	DIO	General-purpose input/output		
GPIO7	30	DIO	General-purpose input/output		
GPIO8	29	DIO	General-purpose input/output		
GPIO9	28	DIO	General-purpose input/output		

RF Antenna Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_WIFI	40	AIO	Wi-Fi antenna interface		50 Ω characteristic impedance.

Control Signals

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
BUSY	10	DO	Power saving	VDD_IO	Externally pulled down to GND with 10 kΩ resistors. If power-saving mode is not used, the pin can not be connected to the host.
WAKEUP_IN	6	DI	Wake up the module	VBAT	If power-saving mode is not used, pull it up to VBAT through a 10 kΩ resistor.

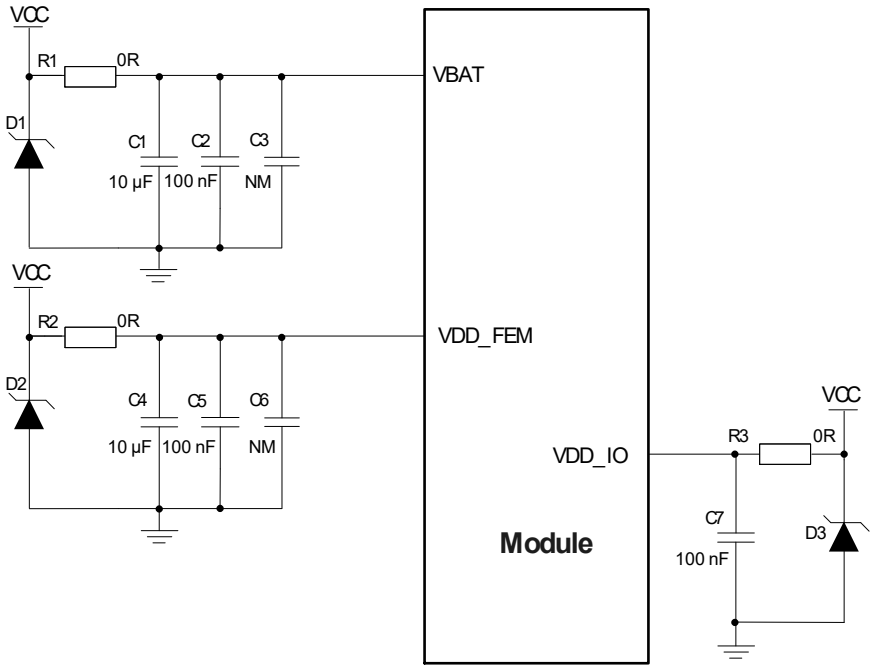
RESET_N	8	DI	Reset the module	Active low.
RESERVED Pins				
Pin Name	**Pin No.**			**Comment**
RESERVED	9, 27, 37			Keep them open.

4.3. Power Supply

The module is powered by VBAT, and the power supply chip for VBAT should provide sufficient current of 0.5 A at least. For better power supply performance, it is recommended to parallel a 10 μF decoupling capacitor and 100 nF filter capacitors near the module's VBAT pin. C3 is reserved for debugging and not mounted by default. In addition, it is recommended to add a TVS near the VBAT to improve the surge voltage bearing capacity of the module. In principle, the longer the VBAT trace is, the wider it should be.

VDD_FEM supplies power for the FEM, and VDD_IO supplies power for the I/O pins of the module. Both power supply designs can be consistent with VBAT's. The circuit reference design is shown below:

Figure 2: Reference Circuit of Power Supply



VBAT, VDD_FEM and VDD_IO do not have strict power-on sequence requirements, but the voltage of VDD_IO should not exceed that of VBAT. In addition, it is necessary to confirm that the level of module power supply interfaces corresponds to the host level.

4.4. Wi-Fi Application Interface

The module provides one SDIO 2.0 interface for Wi-Fi applications. At the same time, the power saving mode can be enabled or disabled by controlling the WAKEUP_IN and BUSY pins.

- If power saving mode is used, a GPIO of the host is needed to be set as a CMOS input pin to receive

the BUSY signal from the pin 10 (BUSY) of the module.

- If power-saving mode is not used, WAKEUP_IN of the module should be pulled up to VBAT through a 10 kΩ resistor. For more details, please contact NetPrisma Technical Support.

The Wi-Fi application interface connection between the module and the host in different modes is shown below:

Figure 3: Wi-Fi Application Interface Connection (Power-Saving Mode)

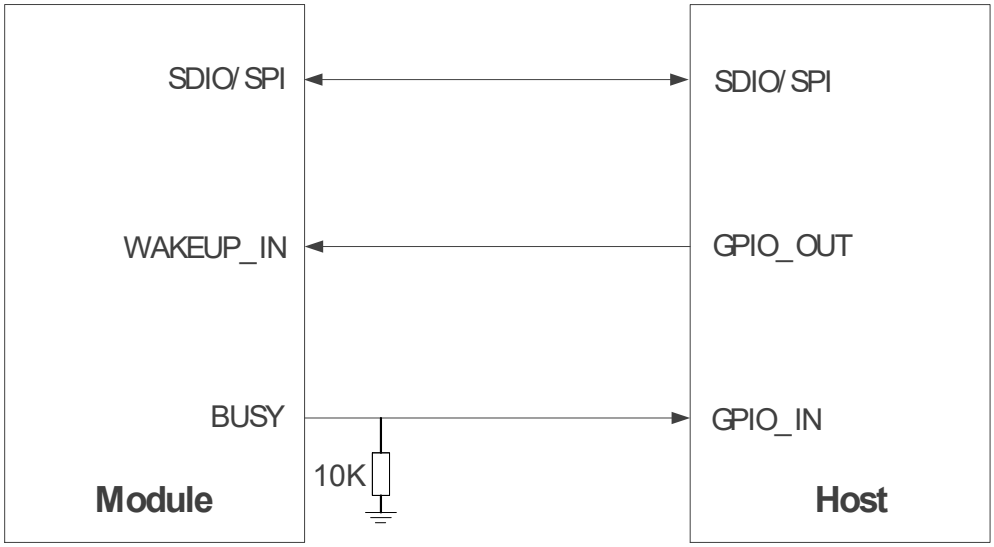
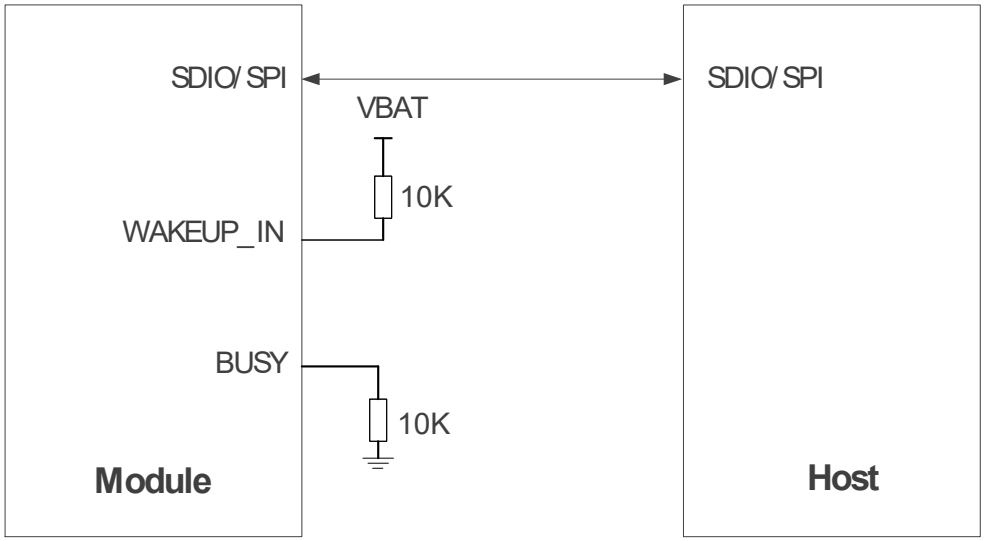


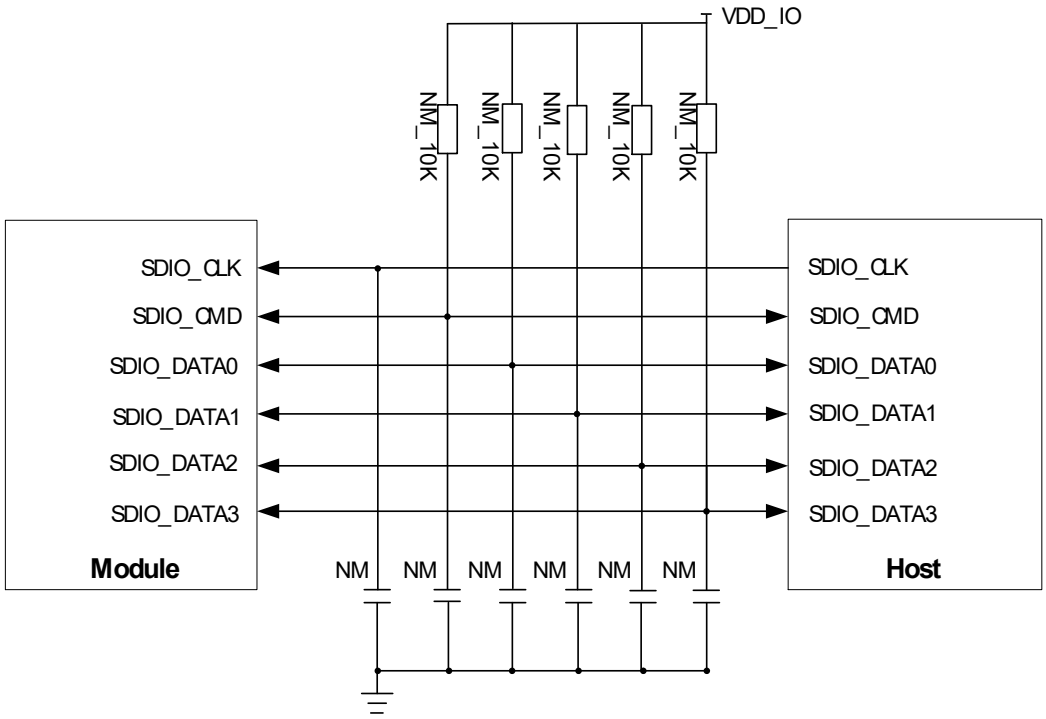
Figure 4: Wi-Fi Application Interface Connection (Non-Power-Saving Mode)



4.4.1. SDIO Interface

In SDIO mode, SDIO interface connection between the module and the host is illustrated in the following figure.

Figure 5: SDIO Interface Connection



To ensure compliance of interface design with the SDIO 2.0 specification, it is recommended to adopt the following principles:

- To avoid jitter of bus, reserve pull-up resistors with value of 10–100 kΩ (recommended value is 10 kΩ) on the SDIO_CMD and SDIO_DATA[0:3] signal traces, and pull them up to VDD_IO of the module.
- The impedance of SDIO signal traces is 50 Ω ±10 %. Route the SDIO traces in inner layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits and analog signals, as well as noise signals such as clock signals and DC-DC signals.
- The distance between SDIO signals and other signals must be greater than twice the trace width, and the bus load capacitance must be less than 15 pF.

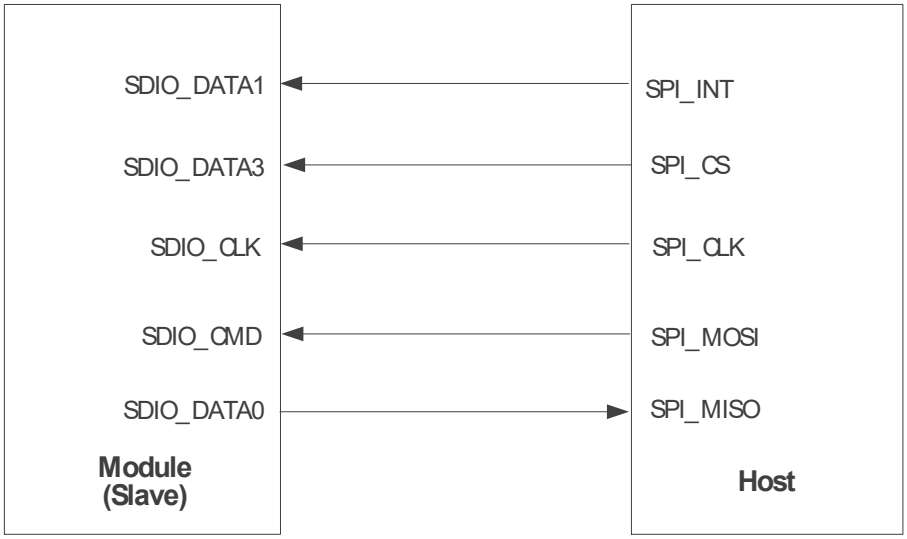
The SDIO interface can be switched to SPI mode by controlling SDIO_DATA3 and SDIO_CMD. Only SPI slave mode is supported. For details, please consult NetPrisma Technical Support. Pull up the unused SDIO_DATA2 to VDD_IO through a 47 kΩ resistor.

Table 7: Pin Description of SDIO Interface in SPI Mode

Pin Name	Pin No.	I/O	Description
SDIO_CLK	24	DI	SPI clock
SDIO_CMD	23	DI	SPI master-out slave-in
SDIO_DATA0	25	DO	SPI master-in slave-out
SDIO_DATA1	26	DI	SPI interrupt
SDIO_DATA3	20	DI	SPI chip select

In SPI mode, SDIO interface connection between the module and the host is illustrated in the following figure.

Figure 6: SDIO Interface Connection in SPI Mode



Consider the following recommendations to achieve the best throughput:

- The host must support level-triggered interrupts.
- The host must support full-duplex mode.
- If the SPI bus requires higher throughput, the host must support DMA transactions. The standard SPI interface has a transmission rate of up to 25 Mbps when the clock frequency is 50 MHz. But if the host does not support DMA transactions, the transmission rate will be significantly reduced. For example, for an SPI interface with an 8-byte DMA transaction buffer, the transfer rate may only reach 2 Mbps.

4.5. JTAG Interface

The module provides a JTAG interface for module testing. JTAG interface is only reset by JTAG_TRST. JTAG_TRST is pulled down to GND with a 10 kΩ resistor inside the module.

4.6. RF Antenna Interface

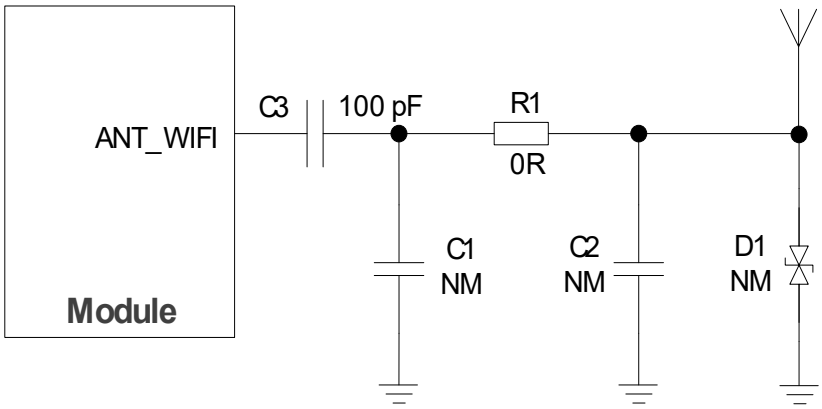
Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module supports one antenna interface (ANT_WIFI). The impedance of antenna port is 50 Ω.

4.6.1. Reference Design

A reference circuit for the RF antenna interface is shown below. It is recommended to reserve a dual L-type circuit and add an ESD protection component for better RF performance. Reserved matching components (R1, C1–C3, and D1) shall be placed as close to the antenna as possible. C1, C2 and D1 are not mounted by default. The parasitic capacitance of TVS should be less than 0.05 pF and R1 is recommended to be 0 Ω.

Figure 7: Reference Circuit for RF Antenna Interface



NOTE

If there is DC power at the antenna port, C3 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C3 should not be reserved.

4.6.2. Requirements for Antenna Design

Table 8: Requirements for Antenna Design

Parameter	Requirement [4]
Frequency Range (MHz)	902–928
Cable Insertion Loss (dB)	< 1
VSWR	≤ 2 (Typ.)
Gain (dBi)	1 (Typ.)
Max. Input Power (W)	50
Input Impedance (Ω)	50
Polarization Type	Vertical

4.6.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

[4] For more details about the RF performances, see ***Chapter 3***.

Figure 8: Microstrip Design on a 2-layer PCB

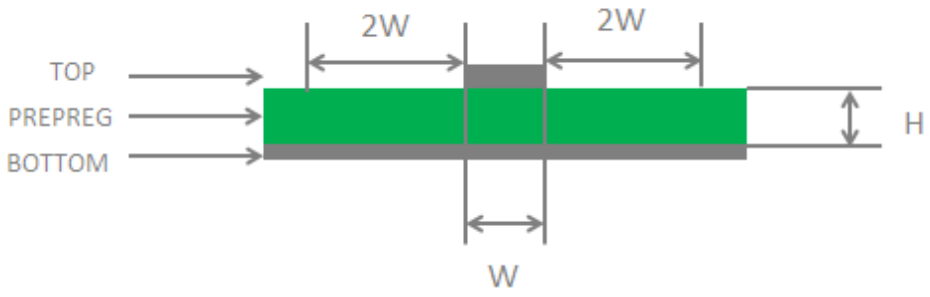


Figure 9: Coplanar Waveguide Design on a 2-layer PCB

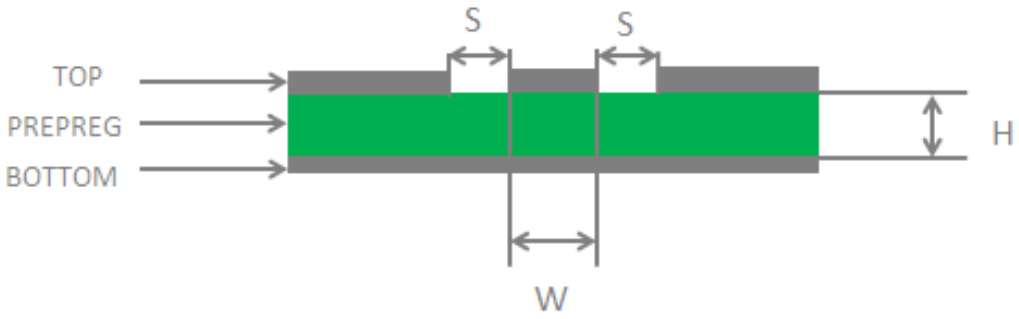


Figure 10: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

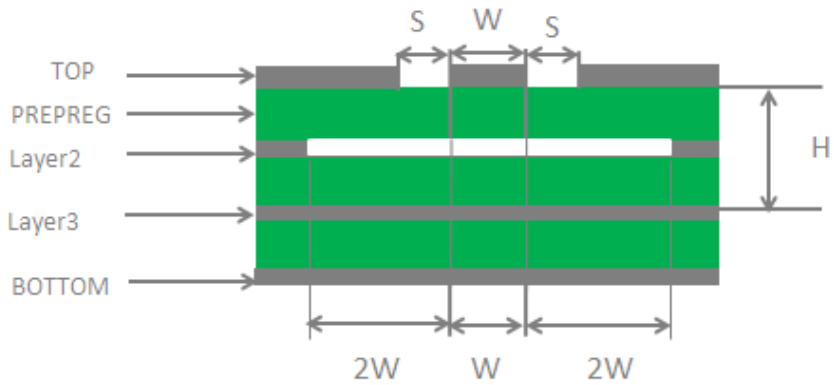
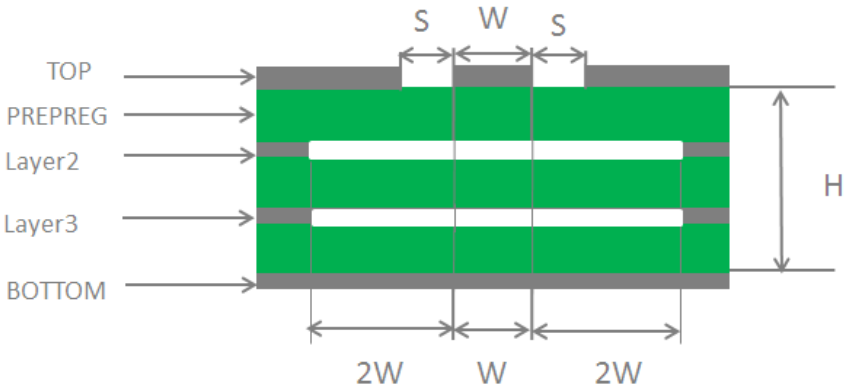


Figure 11: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)



To ensure RF performance and reliability, follow the principles below in RF layout design:

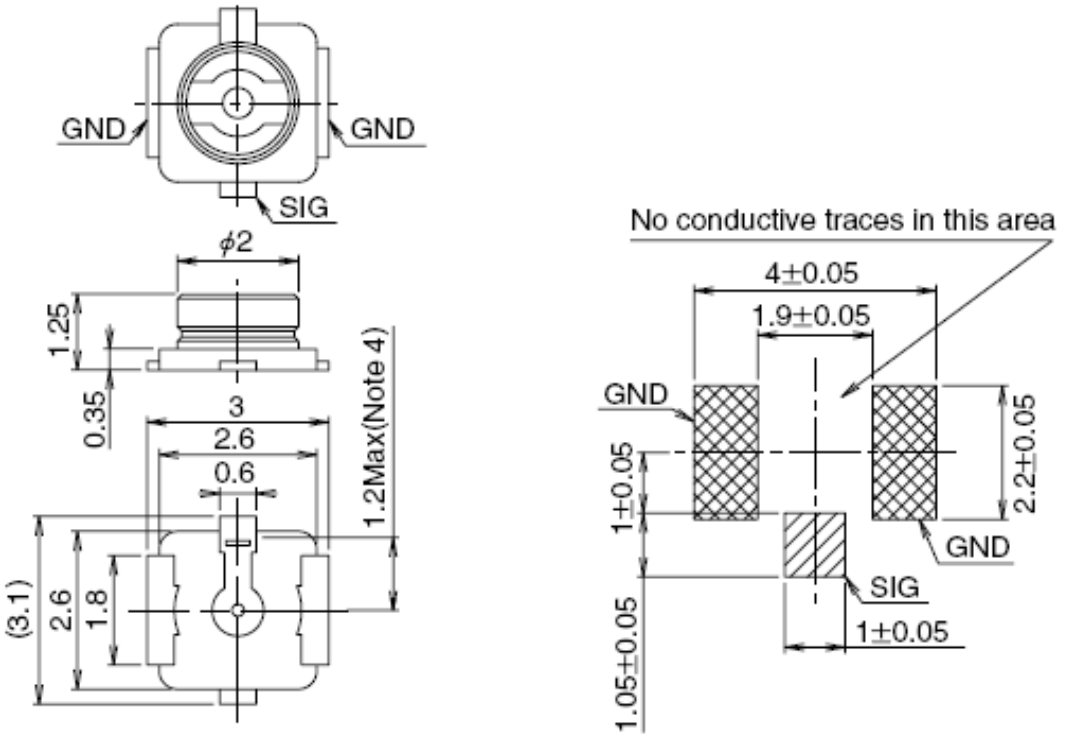
- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The traces of RF pin should be typically routed with ground clearance and have a 50 Ω characteristic impedance.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [2]***.

4.6.4. RF Connector Recommendation

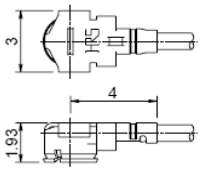
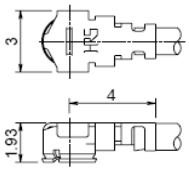
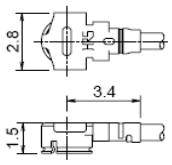
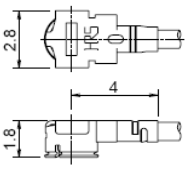
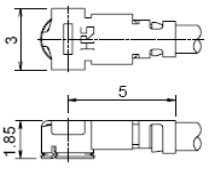
If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

Figure 12: Dimensions of the Receptacle (Unit: mm)



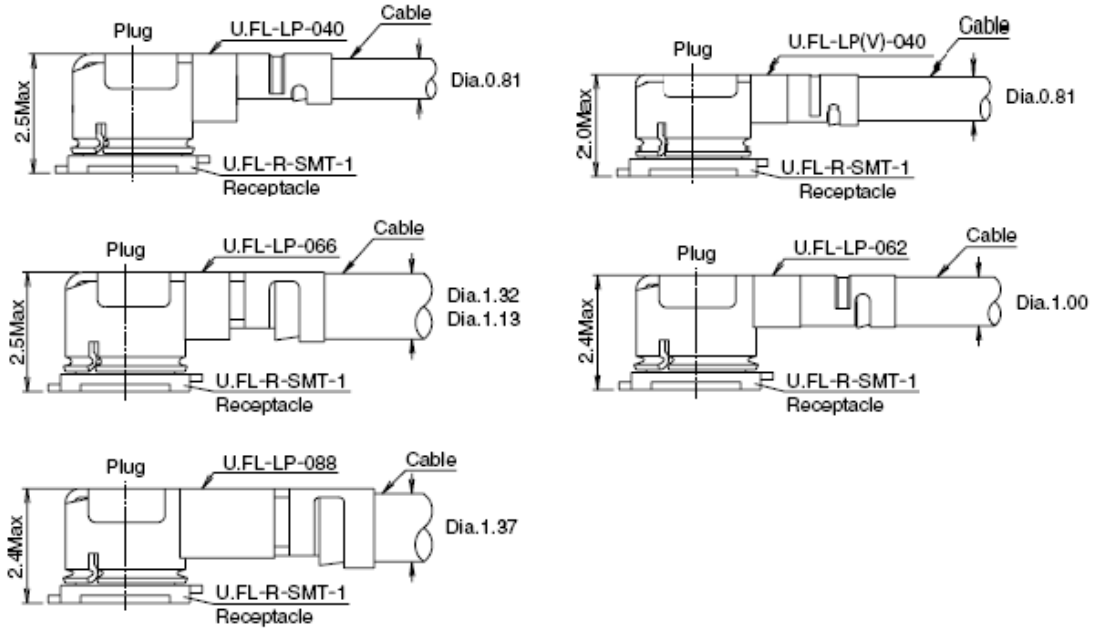
U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

Figure 13: Specifications of Mated Plugs

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

The following figure describes the space factor of mated connectors.

Figure 14: Space Factor of Mated Connectors (Unit: mm)



For more details, please visit http://www.hirose.com.

5 Electrical Characteristics and Reliability

5.1. Absolute Maximum Ratings

Table 9: Absolute Maximum Ratings (Unit: V)

Parameter	Min.	Max.
VBAT	-0.3	4.3
VDD_FEM	-0.3	5.5
VDD_IO	-0.3	4.3

5.2. Power Supply Ratings

Table 10: Module's Power Supply Ratings (Unit: V)

Parameter	Description	Condition	Min.	Typ.	Max.
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	3.0	3.3	3.6
VDD_FEM	Power supply for the FEM	-	3.0	3.3	3.6
VDD_IO	Power supply for I/O pins	-	1.8	3.3	3.6

5.3. Power Consumption

Table 11: Wi-Fi Power Consumption (Typ.; Unit: mA)

Condition		I_{VDD_FEM}	I_{VBAT}
802.11ah, Tx @ 915 MHz	1 MHz @ MCS 0	120	58
	2 MHz @ MCS 0	114	60
	4 MHz @ MCS 0	104	64
	8 MHz @ MCS 0	93	72

	1 MHz @ MCS 7	72	49
	2 MHz @ MCS 7	58	48
	4 MHz @ MCS 7	45	49
	8 MHz @ MCS 7	35	54
	1 MHz @ MCS 10	119	58
802.11ah, Rx @ 915 MHz	1 MHz @ MCS 0	5	27
	2 MHz @ MCS 0	5	29
	4 MHz @ MCS 0	5	36
	8 MHz @ MCS 0	5	42
	1 MHz @ MCS 7	5	29
	2 MHz @ MCS 7	5	31
	4 MHz @ MCS 7	5	36
	8 MHz @ MCS 7	5	43
	1 MHz @ MCS 10	5	28

5.4. Digital I/O Characteristics

Table 12: VDD_IO I/O Requirements (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.7 × VDD_IO	VDD_IO + 0.2
V_{IL}	Low-level input voltage	-0.3	0.3 × VDD_IO
V_{OH}	High-level output voltage	0.9 × VDD_IO	-
V_{OL}	Low-level output voltage	-	0.1 × VDD_IO

5.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

Figure 15: Top and Side Dimensions

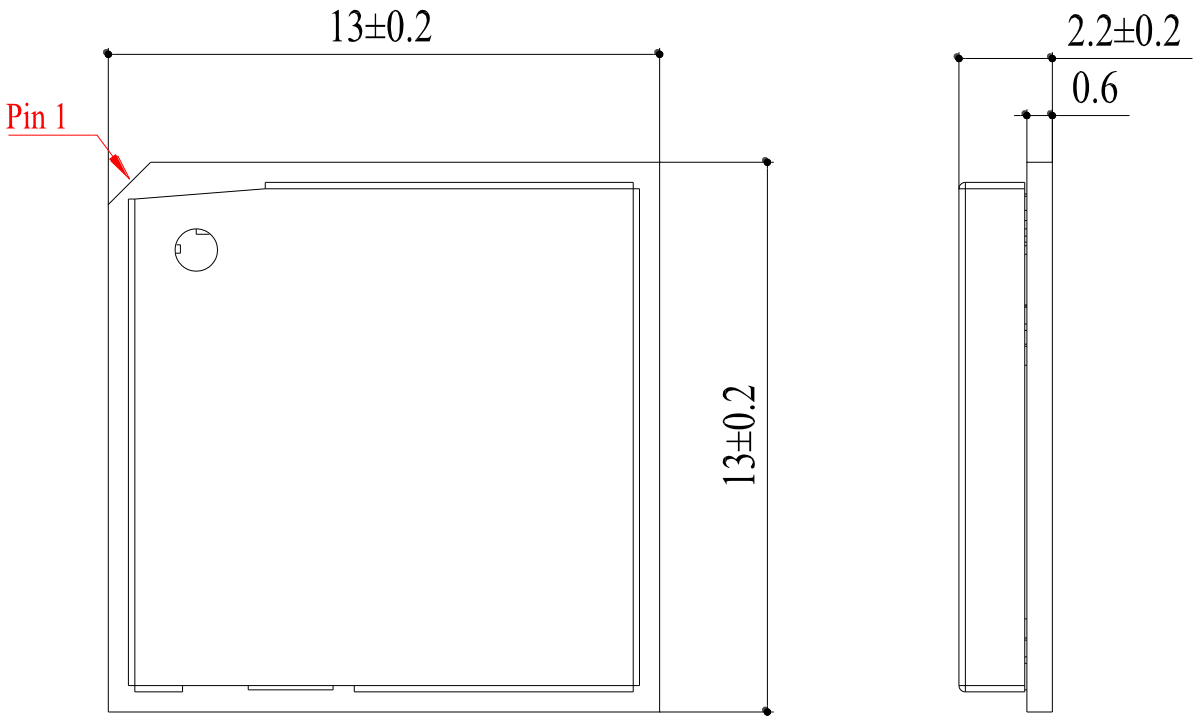
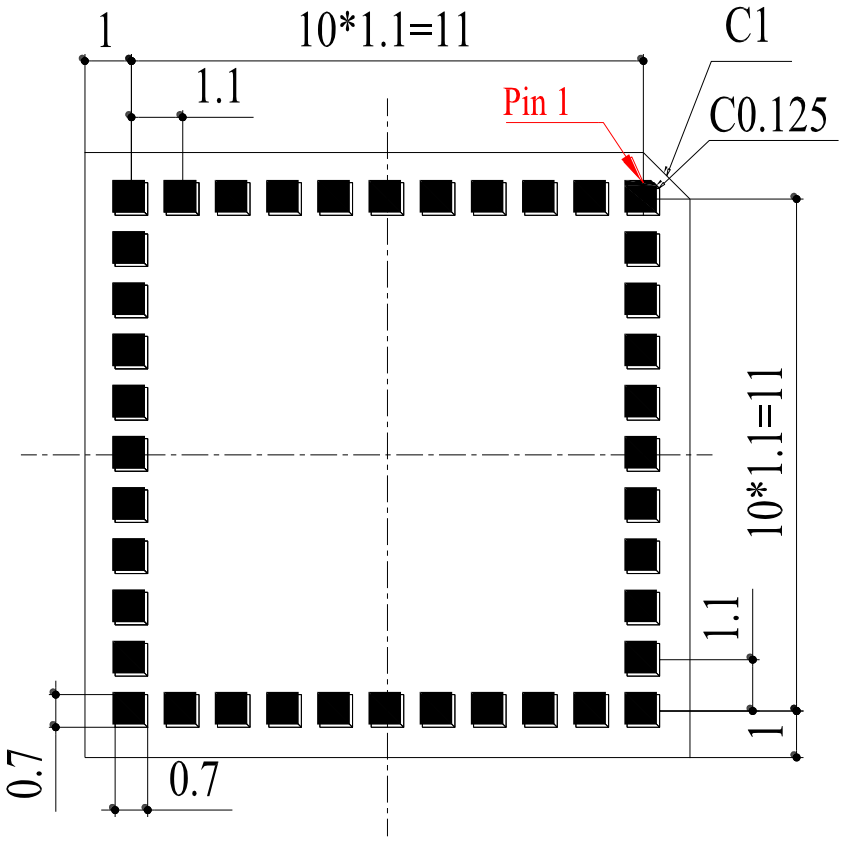


Figure 16: Bottom Dimensions (Bottom View)

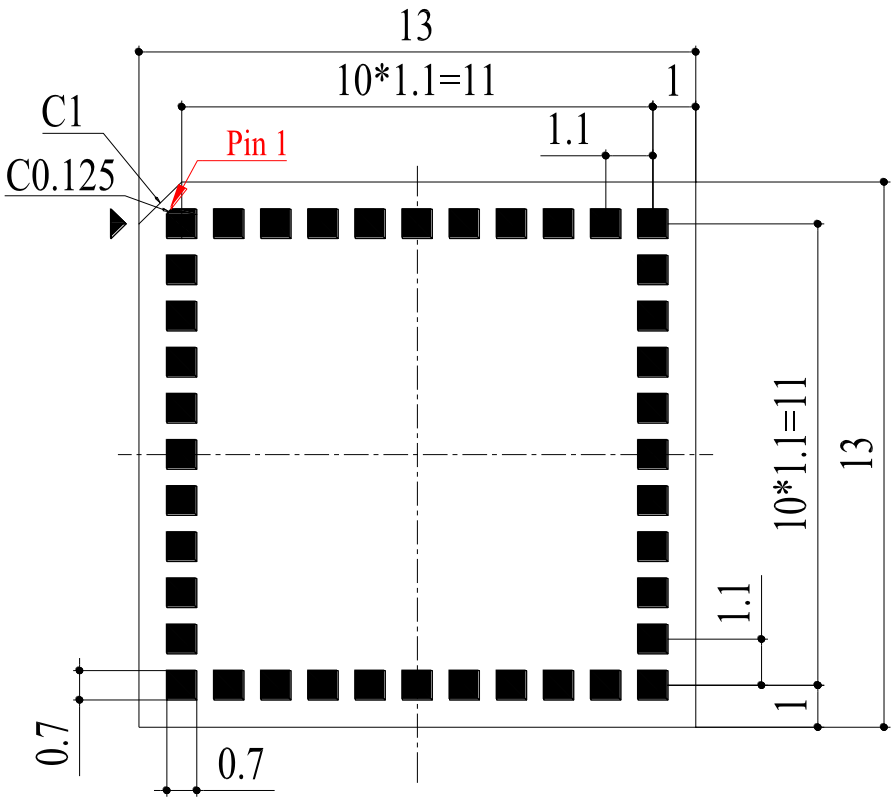


NOTE

The package warpage level of the module refers to *JEITA ED-7306* standard.

6.2. Recommended Footprint

Figure 17: Recommended Footprint

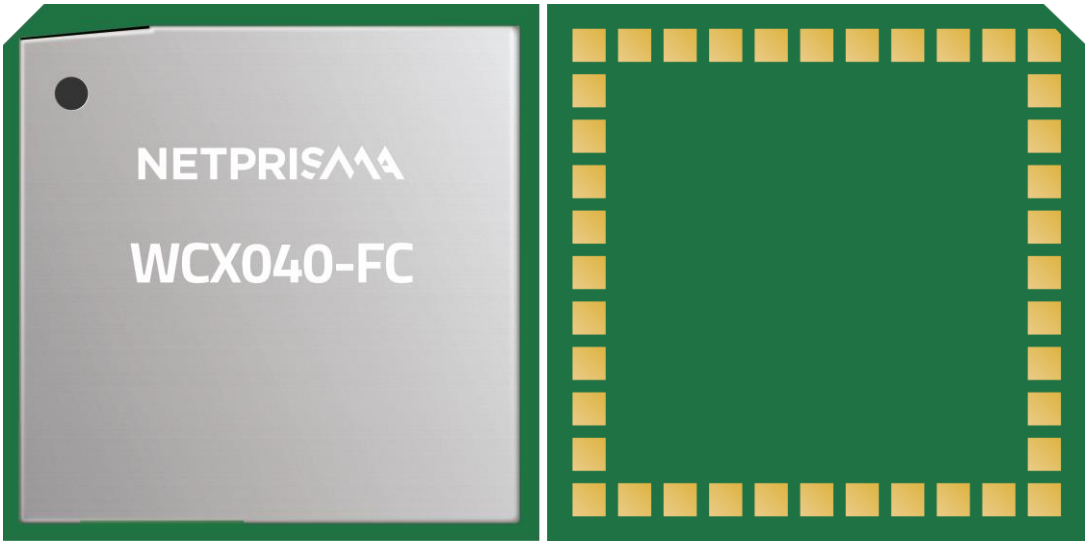


NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

Figure 18: Top and Bottom Views



NOTE

Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from NetPrisma.

7 Storage, Manufacturing and Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [5] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [3]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

[5] This floor life is only applicable when the environment conforms to IPC/JEDEC J-STD-033. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

Figure 19: Recommended Reflow Soldering Thermal Profile

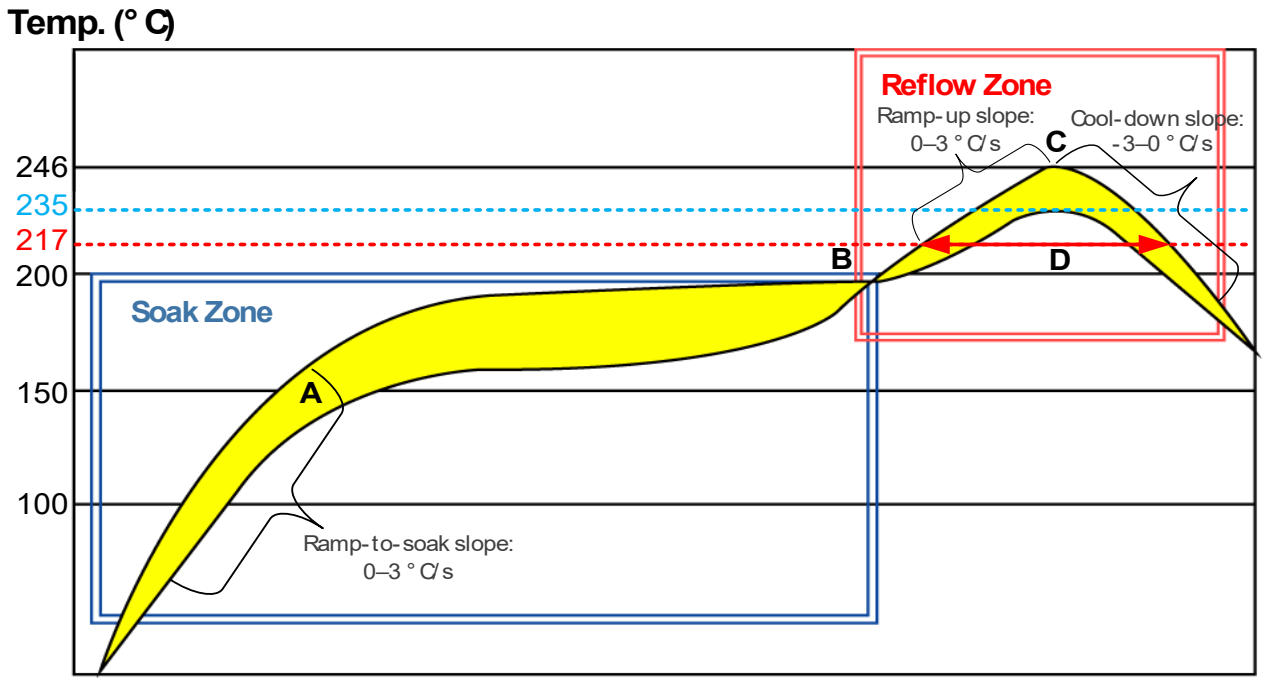


Table 13: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217 °C)	40–70 s
Max. Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max. Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol,

isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, please contact NetPrisma Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

7.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

7.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

Figure 20: Carrier Tape Dimension Drawing (Unit: mm)

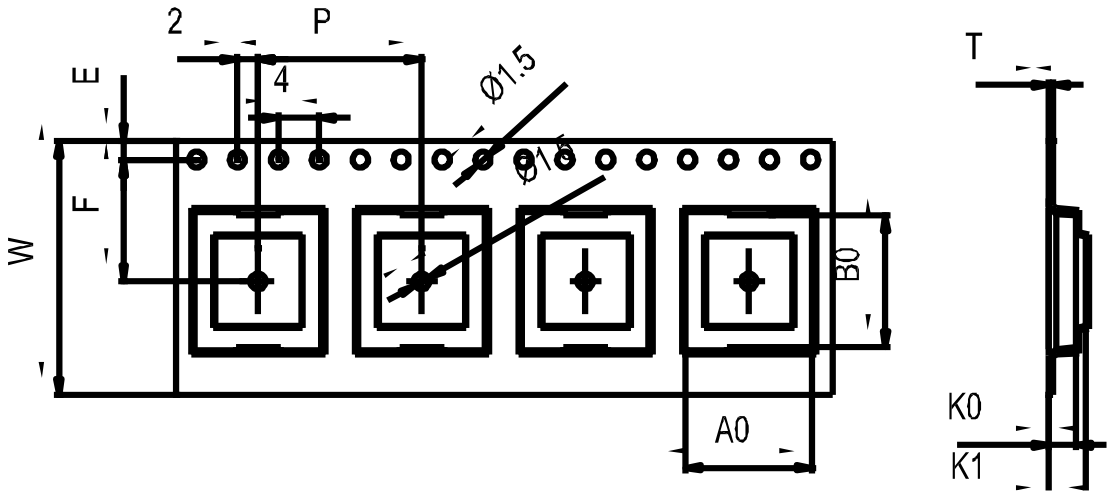


Table 14: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
24	20	0.4	13.4	13.4	2.95	5.6	11.5	1.75

7.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

Figure 21: Plastic Reel Dimension Drawing

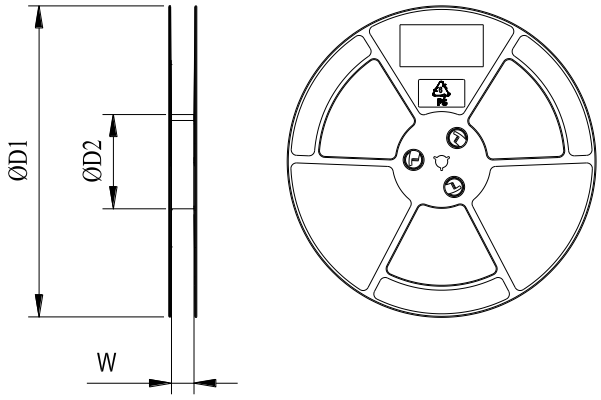
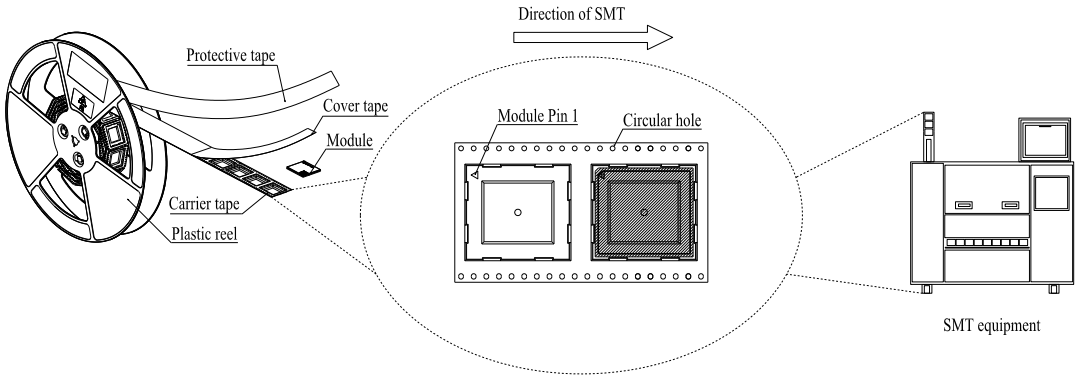


Table 15: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	24.5

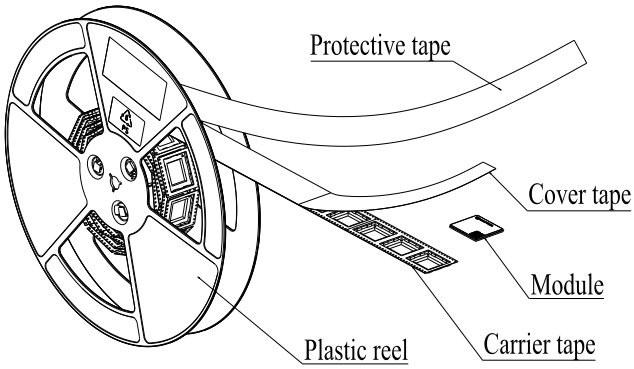
7.3.3. Mounting Direction

Figure 22: Mounting Direction



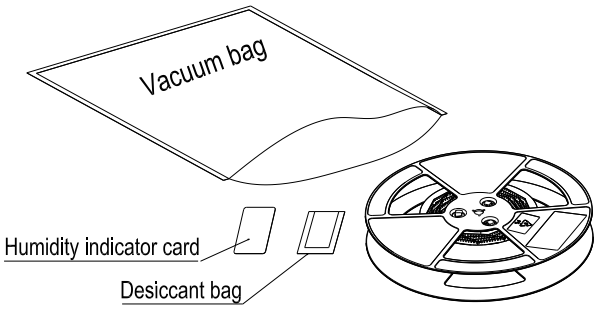
7.3.4. Packaging Process

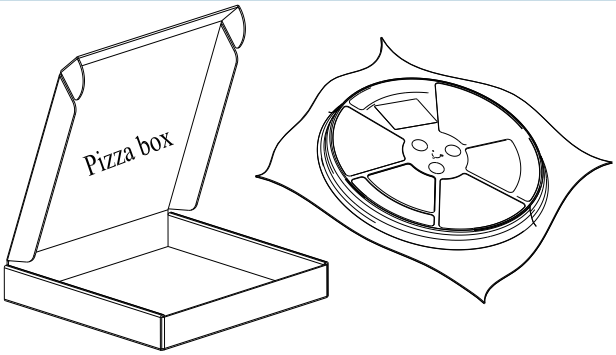
Figure 23: Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

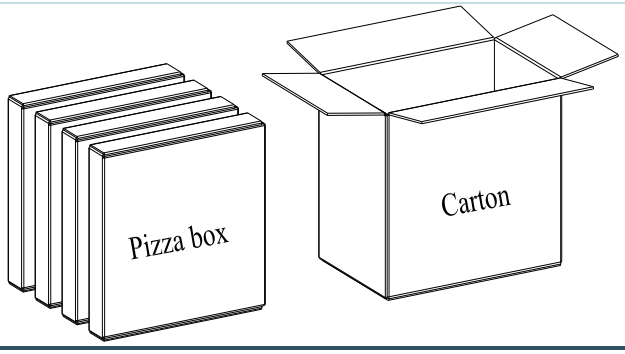
Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.



8 Appendix

Table 16: Related Documents

Document Name
1. NetPrisma-RK3568-WF-EVB-User-Guide
2. NetPrisma-RF-Layout-Application-Note
3. NetPrisma-Module-Stencil-Design-Requirements
4. NetPrism-Module-SMT-Application-Note

Table 17: List of Abbreviations

Abbreviation	Description
AES	Advanced Encryption Standard
AP	Access Point
BPSK	Binary Phase Shift Keying
CCK	Complementary Code Keying
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DMA	Direct Memory Access
ESD	Electrostatic Discharge
EVB	Evaluation Board
EVM	Error Vector Magnitude
FEM	Front-End Module
GND	Ground
GPIO	General-Purpose Input/Output
I/O	Input/Output
IEEE	Institute of Electrical and Electronics Engineers
JTAG	Joint Test Action Group
LGA	Land Grid Array

MBIST	Memory Build-In-Self Test
Mbps	Million Bits Per Second
MCS	Modulation and Coding Scheme
MSL	Moisture Sensitivity Levels
OFDM	Orthogonal Frequency-Division Multiplexing
OWE	Opportunistic Wireless Encryption
PCB	Printed Circuit Board
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RISC-V	Reduced Instruction Set Computer Five
RoHS	Restriction of Hazardous Substances
Rx	Receive
SAW	Surface Acoustic Wave
SDIO	Secure Digital Input/Output
SHA	Secure Hash Algorithm
SMT	Surface Mount Technology
SPDT	Single-Pole Double-Throw
SPI	Serial Peripheral Interface
STA	Station
TVS	Transient Voltage Suppressor
Tx	Transmit
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
Vmax	Maximum Voltage

Vmin	Minimum Voltage
Vnom	Nominal Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WPA	Wi-Fi Protected Access

Document History

Revision	Date	Changes
1.0	2024-08-12	The first major version.

OEM/Integrators Installation Manual

Important Notice to OEM integrators 1. This module is limited to OEM installation ONLY. 2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b). 3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations 4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to NETPRISMA that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID:” 2BEY3WCX040FCA” “Contains IC: “32052-WCX040FCA”. The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 15.247 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:

(1) This device may not cause interference; and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna. As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et

2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 32052-WCX040FCA”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 32052-WCX040FCA ".

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

NETPRISMA INC.
Address: 1301 6TH AVE, SEATTLE, WA, 98101-2304, UNITED STATES
Tel: +1 347 491 2229
Email: info@netprisma.us
Sales support: https://www.netprisma.us/sales-support/

For technical support, or to report documentation errors, please visit:
https://www.netprisma.us/tech-support/
Or email us at: support@netprisma.us