RK3288 Board User manual

1 Document information

This document is the RK3288_UIB_V1.4 hardware design manual.

Table 1 Documentation Modification History

The version number	Modify the content	Head	Modification time
V1.0.1	newly built		2021/11/28

No	The title of the document	Document version	author	illustrate

2 Hardware design block diagram

2.1 Functional block diagram

Figure 1Functional diagram of the RK3288 board circuit

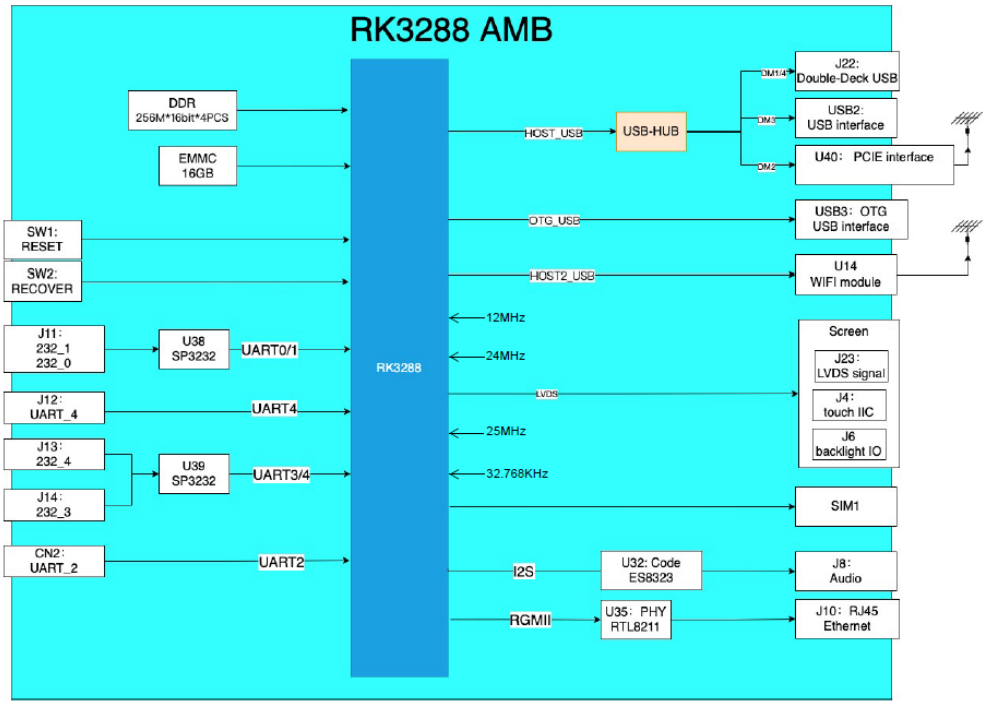
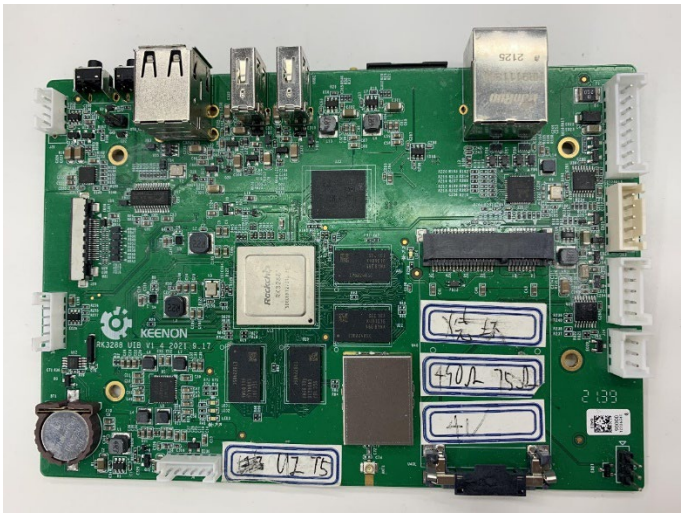
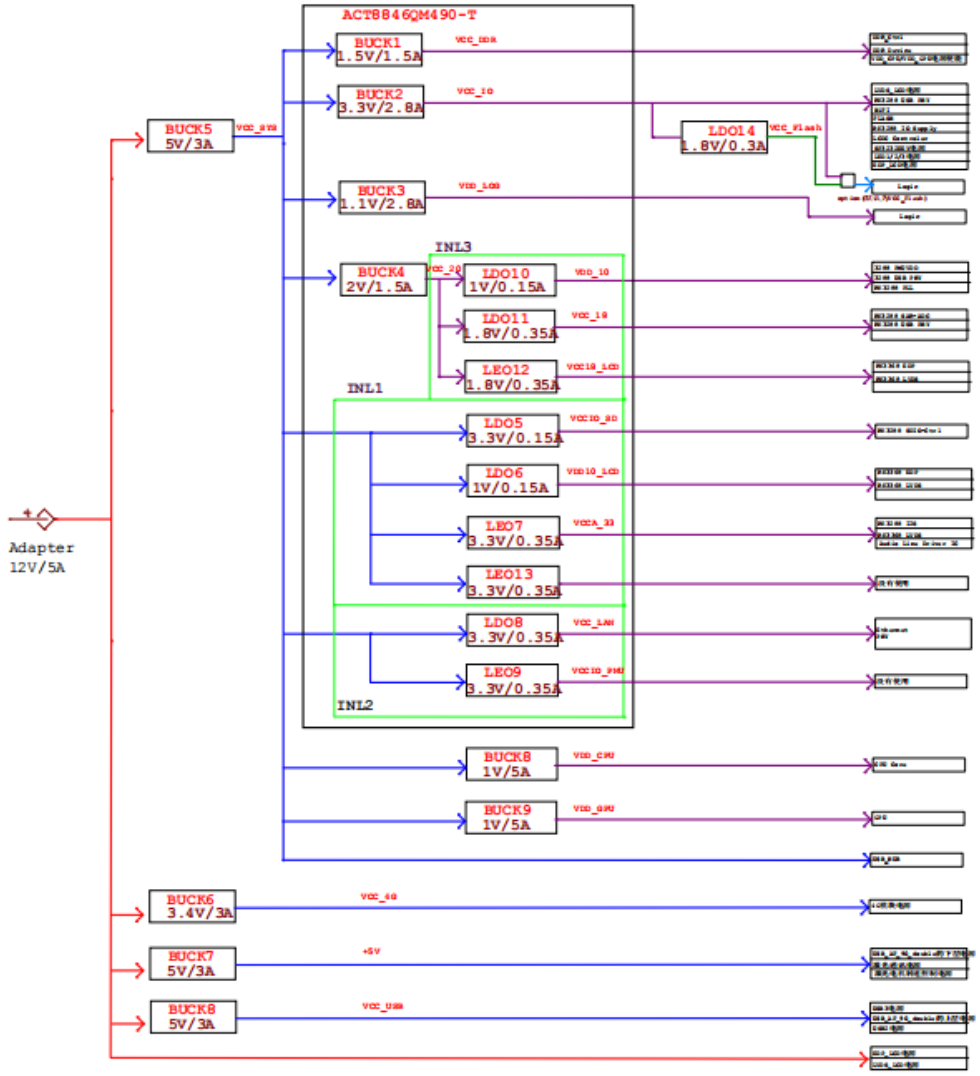


Figure 2 Physical Diagram



2.2 Power diagram

Figure 3 Power Architecture Diagram



3 Power Consumption

Table 2 Power Consumption Table

No	Test conditions	voltage	current	illustrate
1	Board standby power consumption	12V	0.2A	
2	12V maximum output current	12V	1A	

4 Hardware capabilities

4.1 Introduction to the basic functions of the hardware

The RK3288 board mainly has the following functions:

1. 【TEST 1】LCD LCD function:J23,J4,J6 connector and LCD screen connection, for LCD The screen provides a 12V power supply and communicates with it, lights up the LCD screen, and implements touch function
2. 【TEST 2】Output audio function: output MIC audio signal, connect to the amplifier adapter board, drive the horn
3. 【TEST 3】Key reset function:SW1 is the reset button, after pressing, the board resets
4. 【TEST 4】USB communication function:USB interface expanded to four USB,J22 is a dual-layer USB interface, Connect two stereo vision modules,USB3 for external download cables
5. 【TEST 5】Ethernet connection: Ethernet communication function
6. 【TEST 6】RS232 communication function:J11,J13,J14 connectors have RS232 Communication lines
7. 【TEST 7】Serial communication:J12 connector, communication with lidar
8. 【TEST 8】WiFi communication function; communication with WIFI module

4.2 Power supply circuit

Refer to the power architecture diagram:

1. The input 12V voltage of the RK3288 board is provided by the J11 connector;
2. 12V generates VCC_SYS(5V) through DCDC
3. 12V generates VCC_USB(5V) through DCDC
4. 12V generates +5V through DCDC;
5. VCC_SYS(5V) generates a variety of power supplies through the PMU chip;
6. VCC_SYS(5V) generates VDD_CPU by programmable DCDC;
7. VCC_SYS(5V) generates VDD_GPU by programmable DCDC
8. VCC_IO(3.3V) is generated by the LDO VCC_Flash(1.8V).

4.2.1 DCDC:12V to 5V

12V to 5V with THE MP1471's built-in MOS buck DCDC

There are three MP1471 12V to 5V circuits on board

1. VCC_SYS (5V)
   (1) The main on-board 5V supply is supplied to the PMU chip to generate a variety of different voltage value supplies

(2) After two DCDCs,a voltage of 1V is generated, which is supplied to the CPU and GPU respectively

2. VCC-USB（5V）

(1) USB power supply, which is provided to the upper power supply of USB2,USB3 and J22(dual-layer USB).

3. +5V

(1) MoS-controlled provides 5V to the lower layer of power supply to J22(dual-layer USB).

(2) MoS-controlled provides 5V to lidar power

Table 3 DCDC:12V to 5V Function Table

	Functional classes	Feature description	illustrate
1	Input properties	The system input voltage is 4.5V-16Vandnormal operation	YES
2	Output properties	【Demand ID】5V load current	＜3A
3	Output properties	5V Ripple	＜5%
4	Output properties	5V noise	＜3%
5	Output properties	5V Load Regulation	＜10%
6	other	Switching frequency	500KHz
7	other	IO enable	YES
8	Input properties	12V Input Ripple + Noise	<5%
9	Overcurrent protection	Output current exceeds 3Aand overcurrent protection is triggered	YES

Figure 4 DCDC:12V to VCC_SYS(5V)circuit diagram

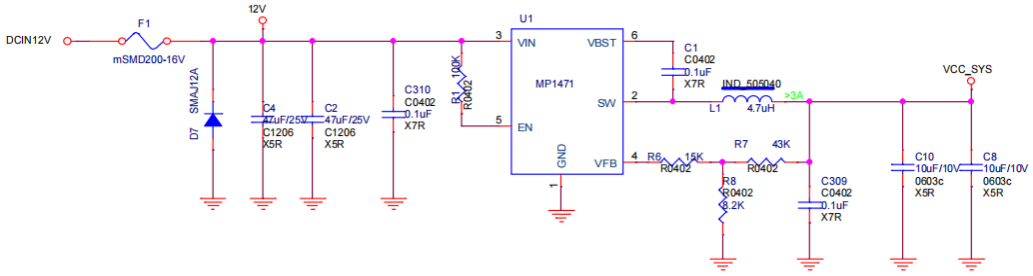


Figure 5 DCDC:12V to VCC-USB(5V))circuit diagram

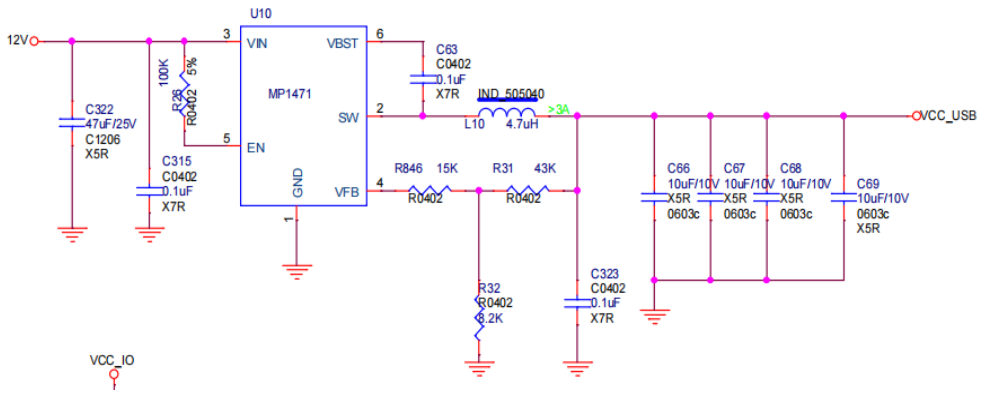
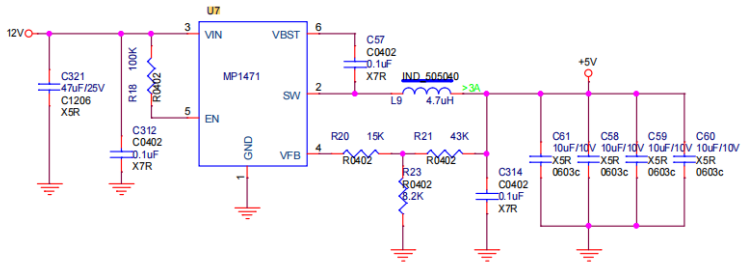


Figure 6 DCDC:12V to +5V Circuit Diagram



4.2.2 PMU:VCC_SYS(5V) generates a variety of power supplies through the PMU chip

The ACT8846QM490-T is a power management chip (PMU) with inputs of VCC_SYS that generate multiple different voltages to supply to the board. There are four DCDCsand nine LDOs. OUT1~OUT4 is the DCDC output,OUT5~OUT13 is the LDO output, and the OUT1 output voltage is adjustable.

Table 5 PMU Input Features Functional Table

	Functional classes	Feature description	illustrate
1	Input properties	The system input voltage is 3.0V-5.5V,normal operation	Yes
2	Input properties	Input Ripple + Noise	<3%

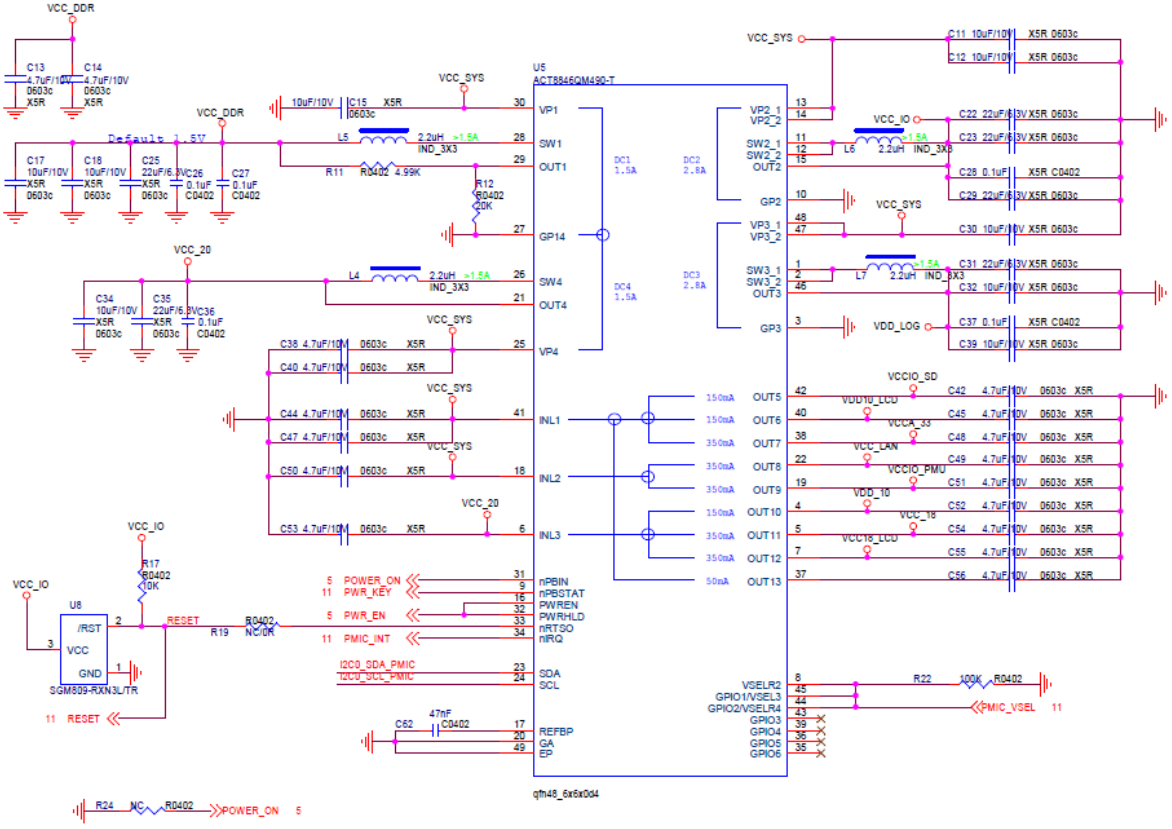
Table 6 PMU(DCDC) Output Features Functional Table

	DCDC output	OUT1	OUT2	OUT3	OUT4
1	Output voltage	1.5V	3.3V	1.0V	2.0V
	Corresponding voltage	VCC_DDR	VCC_IO	VCC_LOG	VCC_20
2	Load current	1.5A	2.8A		1.5A
3	Output ripple + noise	3%			
4	Switching frequency	2.25MHz			
5	other	Voltage adjustable	/	/	/

Table 7 PMU(LDO)Output Features Functional Table

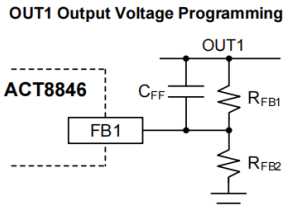
	Output	OUT5	OUT6	OUT7	OUT8	OUT9	OUT10	OUT11	OUT12	OUT13
1	Output voltage	3.3V	1.0V	3.3V	3.3V	3.3V	1.0V	1.8V	1.8V	1.8V
	Corresponding voltage	VCCIO_SD	VDD10_LCD	VCCA_33	VCC_LAN	VCCIO_PMU	VDD_10	VCC_18	VCC18_LCD	/
2	Load current	150mA		350mA			150mA	350mA		50mA
3	other	/								Not used

Figure 8 PMU circuit diagram



The out1 output resistance is determined by the values R11 and R12,R11=4.99K,R12=20k,VFB1=1.2V.
Available,Vout1=(R11/R12+1)*VFB1 = 1.5V

Figure 9 Vout Calculation



$$R_{FB1} = R_{FB2}\left(\frac{V_{OUT1}}{V_{FB1}} - 1\right)$$

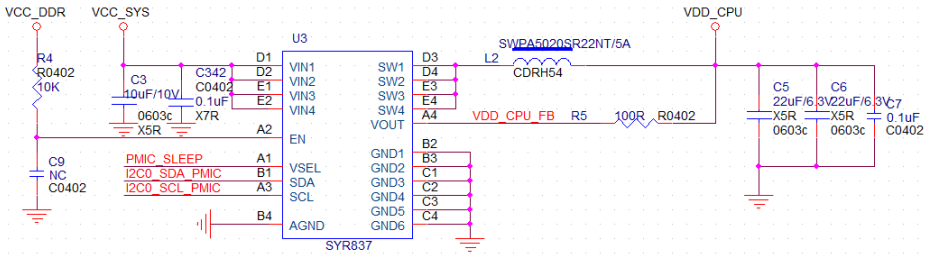
4.2.3 DC:5V to VDD_CPU

VCC_SYS(5V) to VDD_CPU with SYR837 BUCK DCDC. The SYR837 is I2C programmable to regulate the output voltage between 0.7125V and 1.5V.

Table 8 DCDC:5V to VDD_CPU Functional Table

	Functional classes	Feature description	illustrate
1	Input properties	The system input voltage is 2.6V-5.5Vand is normal	YES
2	Output properties	Demand ID: Load current	＜6A
3	Output properties	Ripple + noise	＜5%
6	other	Switching frequency	2.4MHz
7	other	IO enable	YES
8	Input properties	5V Input Ripple + Noise	<5%
9	other	The output voltage is programmable	YES

Figure 10 DCDC:5V to VCC_CPU circuit diagram



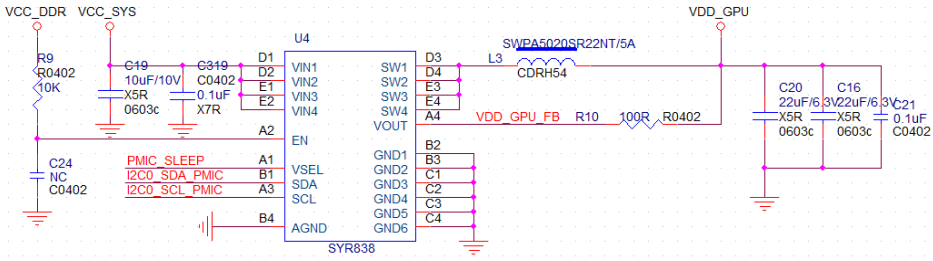
4.2.4 DCDC:5V to VDD_GPU

VCC_SYS(5V) to VDD_GPU with SYR838 BUCK DCDC. The SYR838 is I2C programmable to regulate the output voltage from 0.7125V to 1.5V.

Table 9 DCDC:5V to VDD_GPU Functional Table

	Functional classes	Feature description	illustrate
1	Input properties	The system input voltage is 2.6V-5.5V,normal operation	YES
2	Output properties	Demand ID: Load current	＜6A
3	Output properties	Ripple + noise	＜5%
6	other	Switching frequency	2.4MHz
7	other	IO enable	YES
8	Input properties	5V Input Ripple + Noise	<5%
9	other	The output voltage is programmable	YES

Figure 11 DCDC:5V to VCC_GPU Circuit Diagram



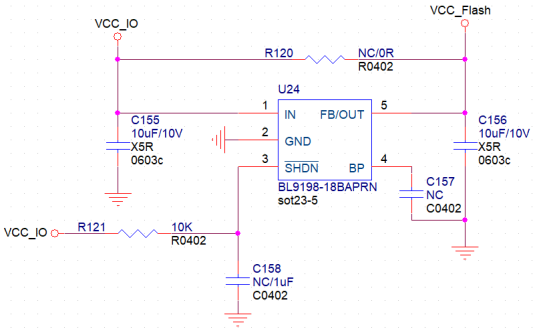
4.2.5 3.3V generates VCC_Flash(1.8V) through the LDO

VCC_IO (3.3V) is generated by DCDC2 of the PMU chip and VCC_Flash by the LDO chip BL9198-18BAPRN to provide to flash circuits.

Table 10 LDO:3.3V to 1.8V Function Table

	Functional classes	Feature description	illustrate
1	Input properties	Input voltage 2V-6V	Yes
2	Output properties	Load current	300mA
3	Output properties	Ripple + noise	＜3%
4	other	With enable	Yes

Figure 12 The LDO circuit



4.3 Minimal system

Uses the RK3288 chip with the following features:

Table 11 Minimum System Feature Table

	Functional classes	Feature description	illustrate
1	Minimal system	Use off-chip 24M crystal oscillators	normal
2	Minimal system	Press the reset button and the board is reset	normal
3	Minimal system	External USB OTG download	normal

4.4 USB circuit

The on-board RK3288 uses a total of three USB channels, namely OTG_USB, HOST1_USB, and HOST2_USB. Each USB power supply is controlled by MOS.

OTG_USB connects to a USB3 connector for external USB download functionality.

HOST1_USB expanded into 4 USB signals via USB_HUB circuit, connected to a dual-layer USB connector (connected to the Stereo Vision Module),USB2 Connector and PCIE interface.

HOST2_USB connect to the WIFI module and communicate with the WiFi module.

Table 12 USB Communication Feature Matrix

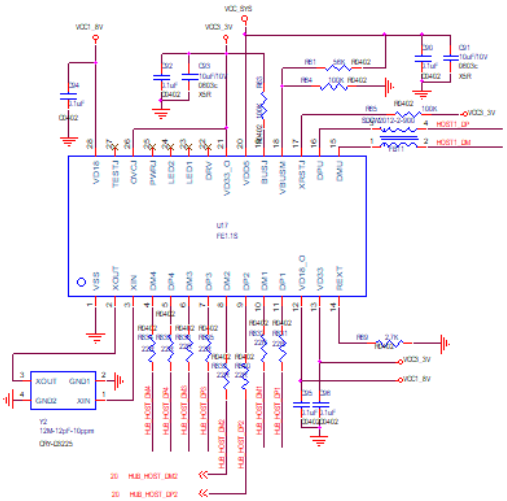
	Functional classes	USB signal	interface	Power Control IO	Instructions for use
1	correspondence	OTG_USB	USB3	OTG_VBUS_DRV	External USB download
2	correspondence	HOST_USB	J22 Upper Floor	DPCAM_PWR	Connect the Stereo Vision module

3	correspondence	Extend 1-4	PCIE interface	/	Communicate with LTE modules
4	correspondence		USB2	HOST1_VBUS_DRV	USB communication
5	correspondence		J22 Lower	HOST_VBUS_DRV	Connect the Stereo Vision module
6	correspondence	HOST2_ USB	WIFI module	USBWIFI_PWR	Communication with WIFI modules

4.4.1 USB_HUB Circuits

The FE1.1S chip extends the HOST1_USB signal to a quad USB signal. Each USB signal is placed in series with a common-mode inductor close to the USB metal interface. DP,DM is the input USB signal,DP1~4,DM1~4 is the extended quad USB Signal. The chip is equipped with a 12M external crystal.

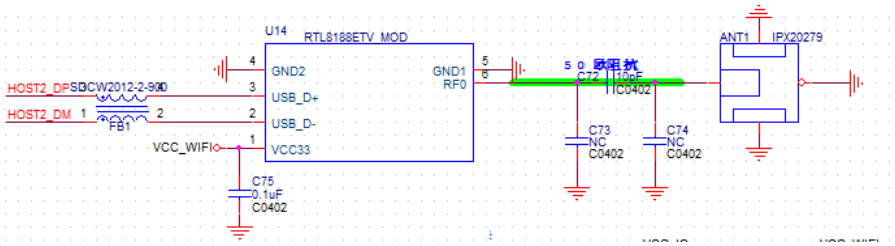
Figure 13 USB_HUB circuit



4.4.2 WIFI circuit

HOST2_USB signal is connected to the RTL8188ETV's WIFI module for communication. The module antenna feeder controls 50 ohm impedance, reserves a Pi-type circuit, and the external chip antenna is connected with an IPX interface. WIFI module custom metal shielding cover, common mode inductance placed close to the module.

Figure 14 WIFI communication circuit

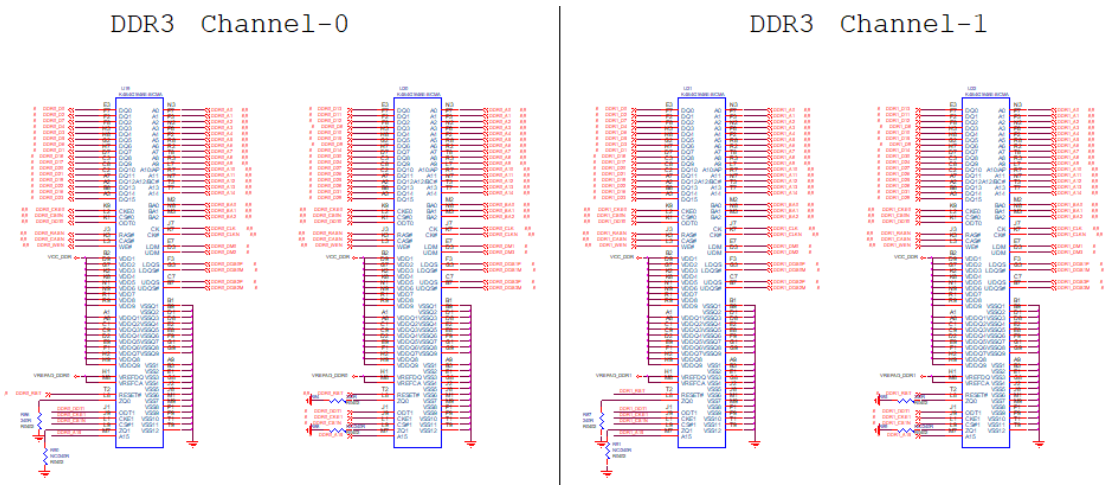


4.5 Storage circuits

4.5.1 DDR Circuits

The board is equipped with four DDR3 SDRAM chips K4B4G1646E-BCMA(256M*16bit), consisting of every two 16-bit chips 256M*32bit,two channels. Chip frequency 933MHz,package FBGA96.

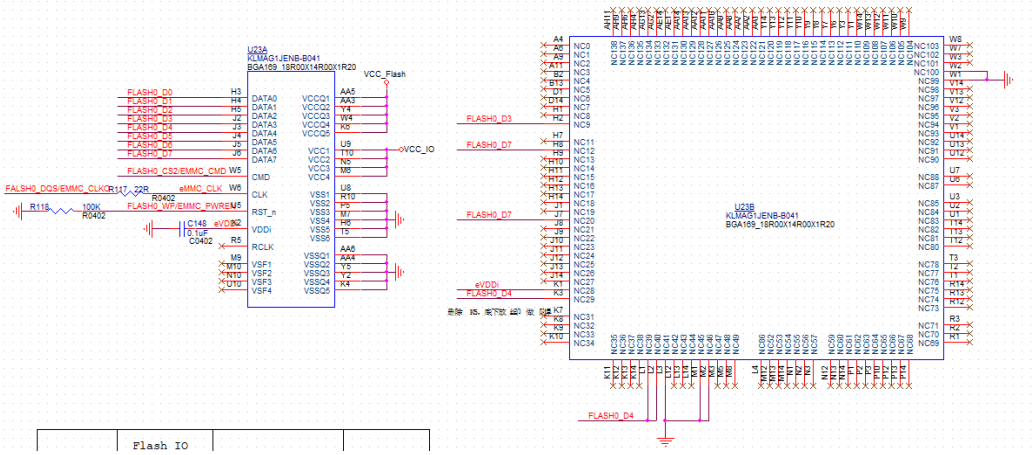
Figure 15 DDR3 circuit



4.5.2 Flash Circuits

The board adopts NAND Flash memory chip KLMAG1JENB-B041,with a capacity of 16GB,a package FBGA169,and a clock frequency of 0~200MHz.

Figure 16 Flash Circuit



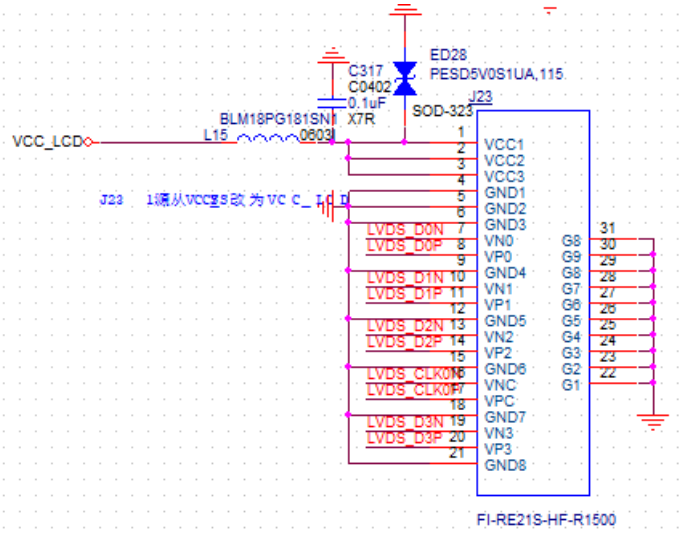
4.6 LCD circuit

The board can drive LCD displays, including LVDS interface,EDP interface, backlight circuitry, and touch circuitry.

4.6.1 LVDS Circuits

The board is equipped with an LVDS interface, with 5 differential signals, connected to the J23 interface output after connecting to the J23 interface output in series, and each set of signal wires is wrapped up and processed for equal length.

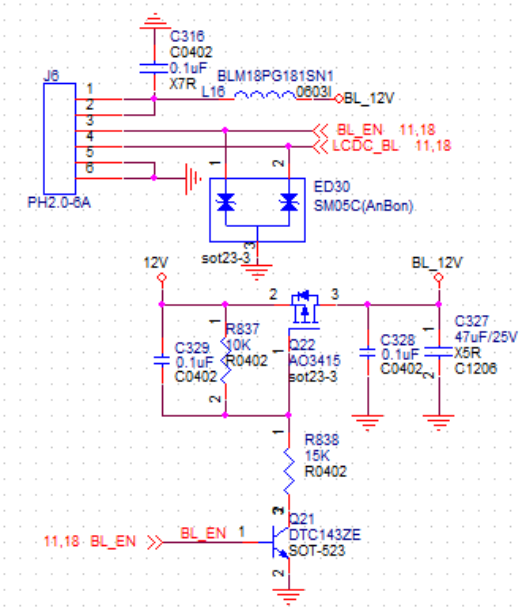
Figure 17 LVDS interface circuit



4.6.2 LCD backlight circuit

LCD supply voltage 12V,controlled output by MOS, control IO to BL_EN.

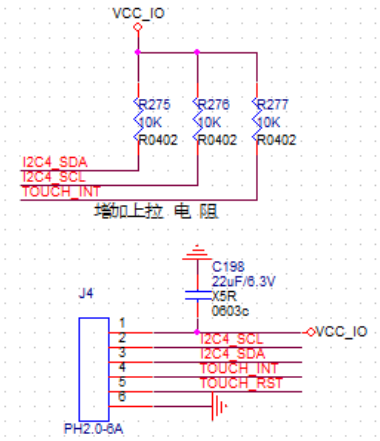
Figure 18 LVDS power and enable interface circuit



4.6.3 Touch Circuits

The J4 is a touchscreen signal connector that communicates with the RK3288 via I2C.

Figure 19 The touch connector circuit



4.6.4 EDP interface

The board is equipped with an EDP interface that communicates with the RK3288 with three differential signals, each connected to the CN1 interface after connecting to the common-mode inductor in series.

Figure 20 EDP output circuit

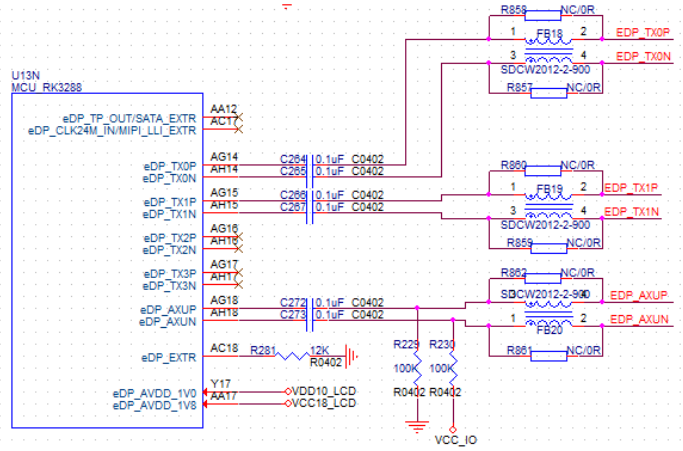
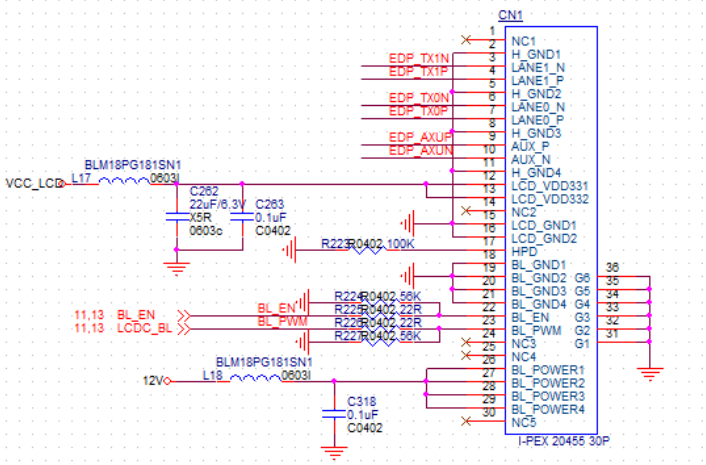


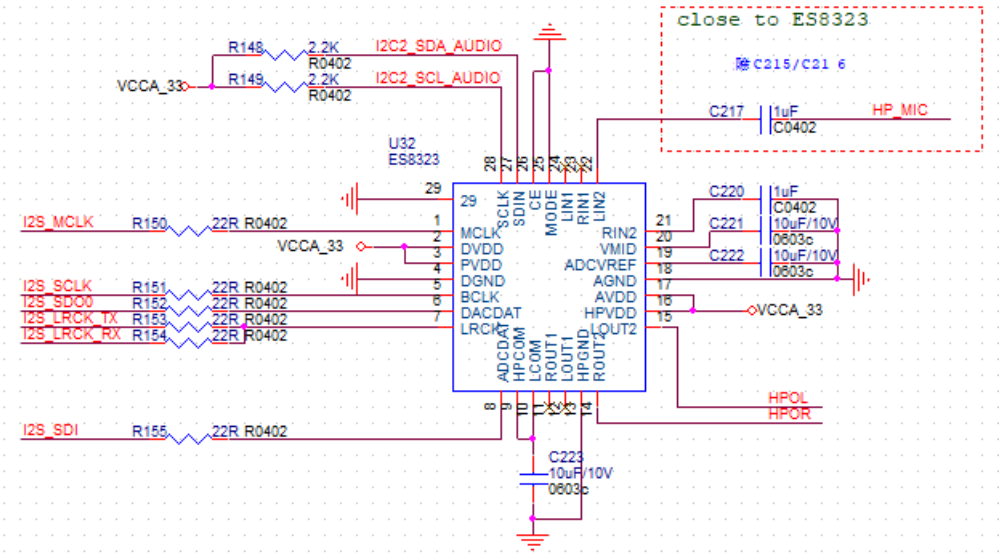
Figure 21 EDP interface circuit



4.7 Audio Circuits

The board is equipped with an audio decoder chip, ES8323(24-bit DAC,8 to 96 kHz sampling frequency), which is used to output audio signals. The ES8323 communicates with the RK3288 via I2S and I2C, HPOL and HPOR is the left and right audio signals of the output.

Figure 22 Audio Circuit



4.8 Ethernet

The RTL8211E-VB-CG is a network transceiver PHY chip that uses an RGMII interface and uses four twisted pair channels for 1000Mbps transmission.

The Gigabit Ethernet physical layer connection path:

RJ45 interface (built-in network isolation transformer)- > network PHY chip - > RK3288(MAC).

Figure 23 Ethernet Interface Circuit

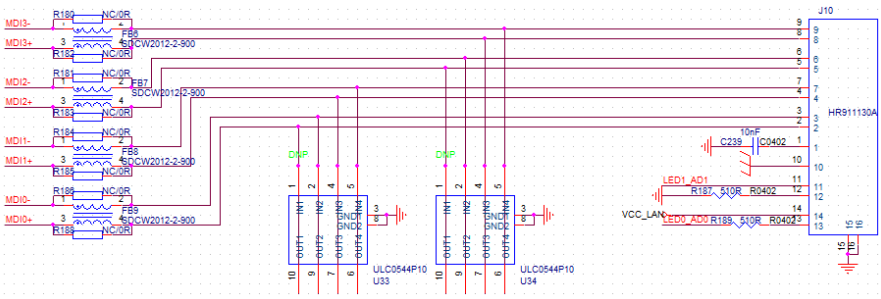
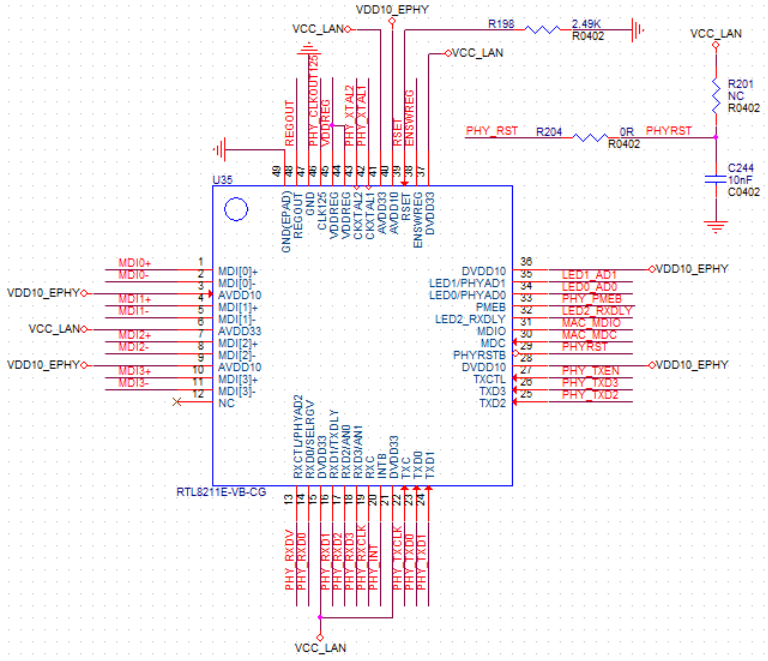


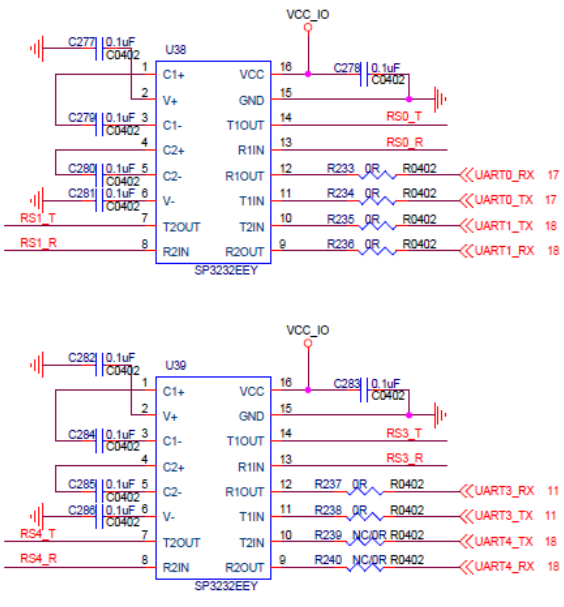
Figure 24 PHY chip circuit



4.9 232 Communication circuits

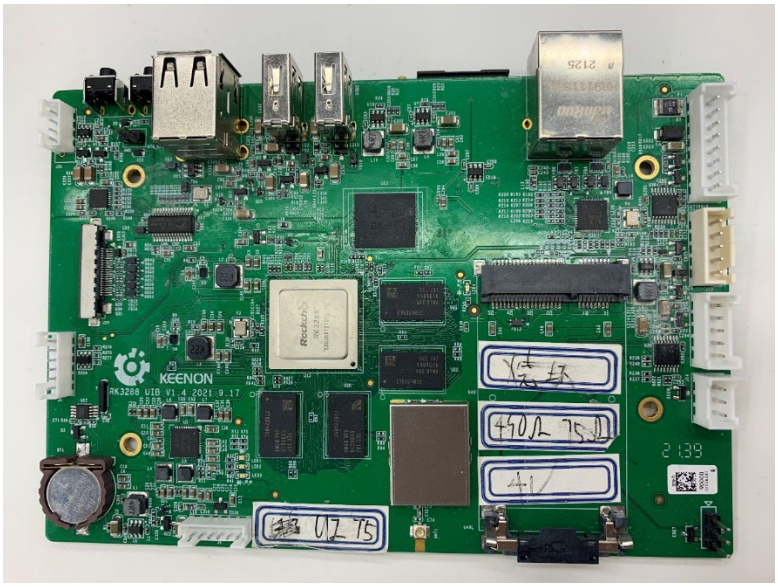
The board has four 232 communication circuits connected to the J11,J13, and J14 connectors to communicate with external devices. The SP3232EEY is a TTL to RS232 level shifting chip with two receivers and two drivers.

Figure 25 232 Circuit



5 Connector datasheet

Figure 28 Physical Diagram



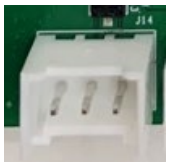
J4:LCD touch interface

Model	HX20020-6A			**Interface Picture:**
description	**HX20020-6A**			
	The network name	**Level**	**current**	**illustrate**
Pin1	VCC_IO	3.3V	2.8A	
Pin2	I2C4_SCL			
Pin3	I2C4_SDA			
Pin4	TOUCH_INT			
Pin5	TOUCH_RST			
Pin6	GND	0V		

J6:LCD backlit interface

Model	PH2.0-6A		**Interface Picture:** 
description	**PH2.0-6A**		
	The network name	**Level**	**illustrate**
Pin1	BL_12V	12V or 0V	
Pin2	BL_12V	12V or 0V	
Pin3	BL_EN		
Pin4	LCDC_BL		
Pin5	GND	0V	
Pin6	GND	0V	

J14:232 Interface 1

Model	HX25037-2A		**Interface Picture:** 
description	**HX25037-3A (Red Star Connector).**		
	The network name	**Level**	**illustrate**
Pin1	RS3_T		
Pin2	RS3_R		
Pin3	GND	0V	

J13:232 Interface 2

Model	HX25037-5A		**Interface Picture:** 
description	**HX25037-5A (Red Star Connector).**		
	The network name	**Level**	**illustrate**
Pin1	LIDA5V	5V or 0V	
Pin2	RS4_R		
Pin3	RS4_T		

Pin4	GND	0V	
Pin5	PWM1		

J12:Serial interface

Model	XH2.54-5P		**Interface Picture:** 
description	**XH2.54-5P**		
	The network name	**Level**	**illustrate**
Pin1	LIDA5V	5V or 0V	
Pin2	UART4_RX		
Pin3	UART4_TX		
Pin4	GND	0V	
Pin5	PWM1		

J11:232 Interface 3

Model	HX25037-8A		**Interface Picture:** 
description	**HX25037-8A (Red Star Connector).**		
	Network Name	**Level**	**illustrate**
Pin1	DCIN12V	12V	input
Pin2	DCIN12V	12V	input
Pin3	GND	0V	
Pin4	GND	0V	
Pin5	RS1_T		
Pin6	RS1_R		
Pin7	RS0_T		
Pin8	RS0_R		

J10:RJ45 interface

Model	HR911130A	**Interface Picture:**

description	Illuminated Gigabit RJ45 network interface socket		
	The network name	**Level**	**illustrate**
Pin1			
Pin2	MDI0+		
Pin3	MDI0-		
Pin4	MDI1+		
Pin5	MDI2+		
Pin6	MDI2-		
Pin7	MDI1-		
Pin8	MDI3+		
Pin9	MDI3-		
Pin10	GND_EARTH	0V	
Pin11	LED1_AD1		
Pin12			
Pin13	LED0_AD0		
Pin14	VCC_LAN	3.3V	
Pin15	GND	0V	
Pin16	GND	0V	

USB2：

Model	USB-AF140PBT		**Interface Picture:** 
description	USBAF side plug three straight foot infinity inner bullet copper 14.0PBT white glue 90 degrees		
	The network name	**Level**	**illustrate**
Pin1	GND	0V	
Pin2	D+	5V or 0V	USB communication cable
Pin3	D-	5V or 0V	USB communication cable
Pin4	5V	5V	
Pin5	GND	0V	
Pin6	GND	0V	
Pin7	GND	0V	

USB3：

Model	USB-AF140PBT		**Interface Picture:** 
description	USBAF side plug three straight foot infinity inner bullet copper 14.0PBT white glue 90 degrees		
	The network name	**Level**	**illustrate**
Pin1	GND	0V	
Pin2	D+	5V or 0V	USB communication cable
Pin3	D-	5V or 0V	USB communication line
Pin4	5V	5V	
Pin5	GND	0V	
Pin6	GND	0V	
Pin7	GND	0V	

J22：

Model	USB_AF_90_double		**Interface Picture:** 
description	USB2-12P-90AF		
	The network name	**Level**	**illustrate**
Pin1	VCC	5V or 0V	
Pin2	D1-	5V or 0V	USB communication cable
Pin3	D1+	5V or 0V	USB communication cable
Pin4	GND	0V	
Pin5	VCC	5V or 0V	
PIN6	D2+	5V or 0V	USB communication cable
Pin7	D2-	5V or 0V	USB communication cable
Pin8	GND	0V	
Pin9	GND	0V	
Pin10	GND	0V	
Pin11	GND	0V	
Pin12	GND	0V	

SW2: Button

Model	keystroke		**Interface Picture:** 
description	6*6*6mm side plug button		
	The network name	**Level**	**illustrate**

Pin1	RECOVER	1.8V or 0V	
Pin2	GND	0V	
Pin3	GND	0V	
Pin4	GND	0V	

SW1：

Model	keystroke		**Interface Picture:** 
description	6*6*6mm side plug button		
	The network name	**Level**	**illustrate**
Pin1	RESET	3.3V or 0V	
Pin2	GND	0V	
Pin3	GND	0V	
Pin4	GND	0V	

J8：

Model	PH2.0-4A		**Interface Picture:** 
description	PH2.0-4A		
	The network name	**Level**	**illustrate**
Pin1	HPL		
Pin2	HP_MIC		
Pin3	GND	0V	
Pin4	HPR		

6 PCB production information

6.1 PCB

Table 14 PCB Size Parameters

Plate size	14.6x10cm		

Number of layers of the board	6	Plate thickness	1.6mm+/-10%
Solder mask color	Blue/Green	Character color	white
Solder mask coverage	Via cover oil	Pad plating	Lead-free OSP
Flying probe test	Test all	Copper thickness	1 oz

Table 15 PCB overlay information

layer	description	typical
TOP	Signal Layer（L1）	1.6
	FR-4	3.8
GND02	GND Layer	1.5
	FR-4	8
ART03	pwr Layer（SIG3）	1.5
	FR-4	30
VCC04	Signal Layer（SIG4）	1.5
	FR-4	8
GND05	GND Layer	1.5
	FR-4	3.8
BOTTOM	Singal Layer（L6）	1.6

Table 16 Impedance Control Table

layer	Single-ended impedance (10± 10%)	Differential impedance (10±10%)		
	50ohm	50ohm	90ohm	100ohm
TOP	4	18mil (refer to layer 3).	5.0/6/5.0	4/4/4
GND02				
ART03	4		5.0/6/5.0	4/4/4
BOTTOM	4		5.0/6/5.0	4/4/4

6.2 PCB Design Rules

6.2.1 Net Class

PCBs are mainly divided into the following categories:

1. Power class
2. Logical classes

6.2.2 Clearance and Creepage

Primary distance information between classes:

1. Between 12V and 12V: 20mil
2. 12V with logic class:20mil

3. Logical classes vs. logical classes:8mil

6.2.3 Additional PCB information

1. The maximum current of the 12V trace is 5A and the minimum width is 100mil
2. TVS,ESD devices as close as possible to the connector
3. LVDS signals, EDP signals, Ethernet PHY signals are controlled with differential impedance control of 100 ohms and USB signal differential impedance control of 90 ohms
4. LVDS signal,EDP signal,PHY signal,DDR signal,Flash signal to do equal length processing, the signal in the group is controlled within 5mil, Different groups of signals are controlled within 100mil
5. The WIFI module antenna feeder is controlled with a 50 ohm impedance
6. The PHY core crystal oscillator should be close to the chip, package processing, and the MAC clock line goes to the inner layer
7. The bottom of the RJ45 connector is cutout
8. The wiring of DCDC needs to consider the loops of dV/dt and dI/dt, reduce the area of the current and voltage mutation loop, and increase the width of the trace
9. 3W:Susceptible to interference and high-speed signals need to be pulled apart at least 3W away from other lines
    (1) Susceptible to interference:Reset,ADC signal
    (2) High-speedsignals:DDR,Flash,PHY signals,DCDC switch pins, crystal oscillators
10. Suture holes: The entire PCB is placed in different GND planes

FCC&IC Statement:

Please take attention that changes or modification not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) This device must accept any interference received, including interference that may cause undesired operation.

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:

(1) this device may not cause interference, and

(2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radioexempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

This equipment complies with FCC/IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

ce matériel est conforme aux limites de dose d'exposition aux rayonnements, FCC / CNR-102 énoncée dans un autre environnement.cette eqipment devrait être installé et exploité avec distance minimale de 20 entre le radiateur et votre corps.

The device must not be co-located or operating in conjunction with any other antenna or transmitter, except in accordance with FCC/IC multi-transmitter evaluation procedures.