GEE811

Datasheet Version 1.0

2.4 GHz Wi-Fi (802.11b/g/n) and Bluetooth® 5 module
Built around ESP32-S3 series of SoCs, Xtensa® dual-core 32-bit LX7 microprocessor
Flash up to 16 MB, PSRAM up to 16 MB
Up to 36 GPIOs, rich set of peripherals
On-board PCB antenna

1 Module Overview

1.1 Features

CPU and On-Chip Memory

- ESP32-S3 series of SoCs embedded, Xtensa® dual-core 32-bit LX7 microprocessor (with single precision FPU), up to 240 MHz
- 384 KB ROM
- 512 KB SRAM
- 16 KB SRAM in RTC
- Up to 16 MB PSRAM

Wi-Fi

- 802.11b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412 ~ 2462MHz

Bluetooth

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

Peripherals

- 36 GPIOs
  - 4 strapping GPIOs
- SPI, LCD interface, Camera interface, UART, I2C, I2S, remote control, pulse counter, LED PWM, full-speed USB 2.0 OTG, USB Serial/JTAG controller, MCPWM, SDIO host controller, GDMA, TWAI® controller (compatible with ISO 11898-1), ADC, touch sensor, temperature sensor, timers and watchdogs

Integrated Components on Module

- 40 MHz crystal oscillator
- Up to 16 MB Quad SPI flash

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating ambient temperature:
  - 65 °C version: –40 ~ 65 °C
  - 85 °C version: –40 ~ 85 °C

Application Scenarios

- Hardware for Intelligent Agent
- LLM Dialogue Systems
- Smart Toys

Contents

2 Block Diagram

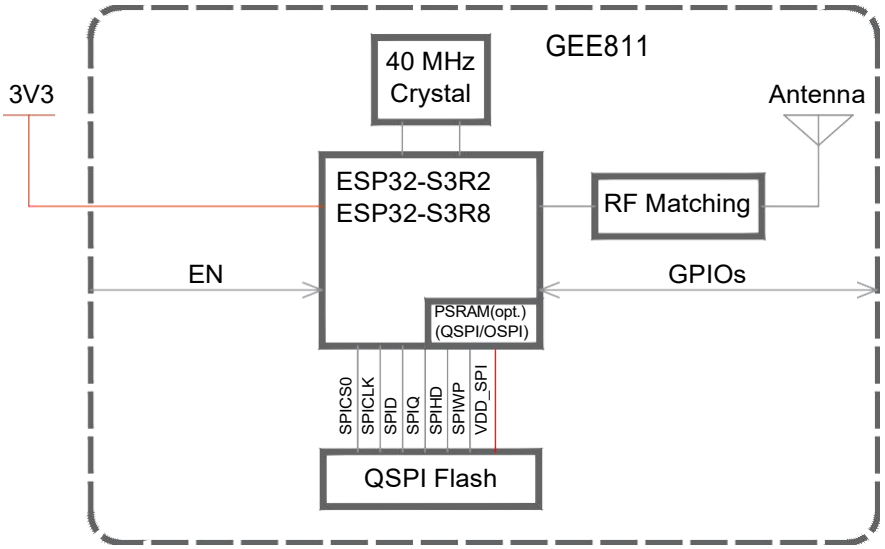

Figure 1: GEE811 Block Diagram

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure Module Dimensions.

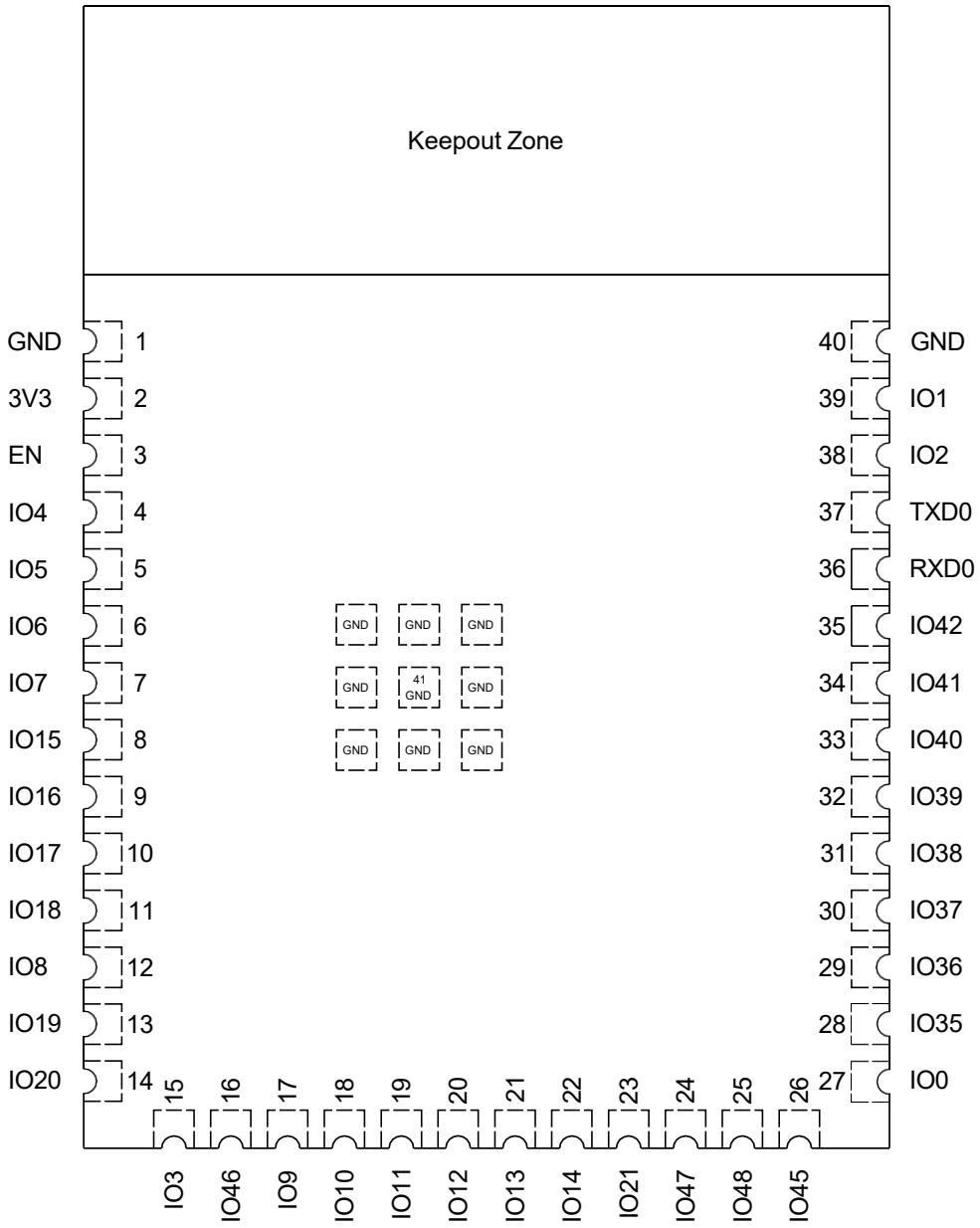

Figure 3: Pin Layout (Top View)

32 Pin Description

The module has 41 pins. See pin definitions in Table 3 *Pin Definitions*.

For explanations of pin names and function names, as well as configurations of peripheral pins, please refer to *ESP32-S3 Series Datasheet*.

Table 3: Pin Definitions

Name	No.	Type [a]	Function
GND	1	P	GND
3V3	2	P	Power supply
EN	3	I	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the EN pin floating.
IO4	4	I/O/T	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
IO5	5	I/O/T	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
IO6	6	I/O/T	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
IO7	7	I/O/T	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
IO15	8	I/O/T	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
IO16	9	I/O/T	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
IO17	10	I/O/T	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6
IO18	11	I/O/T	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, CLK_OUT3
IO8	12	I/O/T	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7, SUBSPICS1
IO19	13	I/O/T	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
IO20	14	I/O/T	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
IO3	15	I/O/T	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
IO46	16	I/O/T	GPIO46
IO9	17	I/O/T	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPIHD, SUBSPIHD
IO10	18	I/O/T	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4, SUBSPICS0
IO11	19	I/O/T	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID, FSPIIO5, SUBSPID
IO12	20	I/O/T	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6, SUBSPICLK
IO13	21	I/O/T	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7, SUBSPIQ
IO14	22	I/O/T	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS, SUBSPIWP
IO21	23	I/O/T	RTC_GPIO21, GPIO21
IO47 [c]	24	I/O/T	SPICLK_P_DIFF,GPIO47, SUBSPICLK_P_DIFF
IO48 [c]	25	I/O/T	SPICLK_N_DIFF,GPIO48, SUBSPICLK_N_DIFF
IO45	26	I/O/T	GPIO45
IO0	27	I/O/T	RTC_GPIO0, GPIO0
IO35 [b]	28	I/O/T	SPIIO6, GPIO35, FSPID, SUBSPID
IO36 [b]	29	I/O/T	SPIIO7, GPIO36, FSPICLK, SUBSPICLK
IO37 [b]	30	I/O/T	SPIDQS, GPIO37, FSPIQ, SUBSPIQ
IO38	31	I/O/T	GPIO38, FSPIWP, SUBSPIWP

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Table 3 – cont'd from previous page

Name	No.	Type [a]	Function
IO39	32	I/O/T	MTCK, GPIO39, CLK_OUT3, SUBSPICS1
IO40	33	I/O/T	MTDO, GPIO40, CLK_OUT2
IO41	34	I/O/T	MTDI, GPIO41, CLK_OUT1
IO42	35	I/O/T	MTMS, GPIO42
RXD0	36	I/O/T	U0RXD, GPIO44, CLK_OUT2
TXD0	37	I/O/T	U0TXD, GPIO43, CLK_OUT1
IO2	38	I/O/T	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
IO1	39	I/O/T	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
GND	40	P	GND
EPAD	41	P	GND

[a] P: power supply; I: input; O: output; T: high impedance. Pin functions in bold font are the default pin functions. For pin 28 ~ 30, the default function is decided by eFuse bit.

[b] For modules with Octal SPI PSRAM, i.e., modules embedded with ESP32-S3R8 or ESP32-S3R16V, pins IO35, IO36, and IO37 are connected to the Octal SPI PSRAM and are not available for other uses.

[c] For modules embedded with ESP32-S3R16V, as the VDD_SPI voltage of the ESP32-S3R16V chip is set to 1.8 V, the working voltage for GPIO47 and GPIO48 is also 1.8 V, which is different from other GPIOs.

4 Boot Configurations

Note:
The content below is excerpted from *ESP32-S3 Series Datasheet* > Section *Boot Configurations*. For the strapping pin mapping between the chip and modules, please refer to Chapter 8 *Module Schematics*.

The chip allows for configuring the following boot parameters through strapping pins and eFuse bits at power-up or a hardware reset, without microcontroller interaction.

- Chip boot mode
  - Strapping pin: GPIO0 and GPIO46
- VDD_SPI voltage
  - Strapping pin: GPIO45
  - eFuse parameter: EFUSE_VDD_SPI_FORCE and EFUSE_VDD_SPI_TIEH
- ROM message printing
  - Strapping pin: GPIO46
  - eFuse parameter: EFUSE_UART_PRINT_CONTROL and EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT
- JTAG signal source
  - Strapping pin: GPIO3
  - eFuse parameter: EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_STRAP_JTAG_SEL

The default values of all the above eFuse parameters are 0, which means that they are not burnt. Given that eFuse is one-time programmable, once programmed to 1, it can never be reverted to 0. For how to program eFuse parameters, please refer to *ESP32-S3 Technical Reference Manual* > Chapter *eFuse Controller*.

The default values of the strapping pins, namely the logic levels, are determined by pins' internal weak pull-up/pull-down resistors at reset if the pins are not connected to any circuit, or connected to an external high-impedance circuit.

Table 4: Default Configuration of Strapping Pins

Strapping Pin	Default Configuration	Bit Value
GPIO0	Weak pull-up	1
GPIO3	Floating	–
GPIO45	Weak pull-down	0
GPIO46	Weak pull-down	0

To change the bit values, the strapping pins should be connected to external pull-down/pull-up resistances. If the ESP32-S3 is used as a device by a host MCU, the strapping pin voltage levels can also be controlled by the host MCU.

All strapping pins have latches. At system reset, the latches sample the bit values of their respective strapping pins and store them until the chip is powered down or shut down. The states of latches cannot be changed in

any other way. It makes the strapping pin values available during the entire chip operation, and the pins are freed up to be used as regular IO pins after reset.

The timing of signals connected to the strapping pins should adhere to the *setup time* and *hold time* specifications in Table 5 and Figure 4.

Table 5: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_H	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

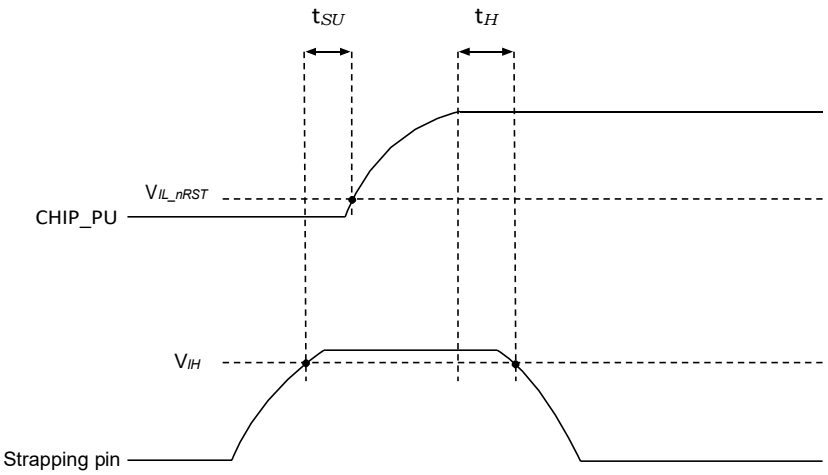

Figure 4: Visualization of Timing Parameters for the Strapping Pins

4.1 Chip Boot Mode Control

GPIO0 and GPIO46 control the boot mode after the reset is released. See Table 6 *Chip Boot Mode Control*.

Table 6: Chip Boot Mode Control

Boot Mode	GPIO0	GPIO46
SPI Boot	1	Any value
Joint Download Boot [2]	0	0

[1] Bold marks the default value and configuration.

[2] Joint Download Boot mode supports the following download methods:

- USB Download Boot:
  - USB-Serial-JTAG Download Boot
  - USB-OTG Download Boot
- UART Download Boot

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system.

In Joint Download Boot mode, users can download binary files into flash using UART0 or USB interface. It is also possible to download binary files into SRAM and execute it from SRAM.

In addition to SPI Boot and Joint Download Boot modes, ESP32-S3 also supports SPI Download Boot mode. For details, please see *ESP32-S3 Technical Reference Manual* > Chapter *Chip Boot Control*.

42 VDD_SPI Voltage Control

Depending on the value of EFUSE_VDD_SPI_FORCE, the voltage can be controlled in two ways.

Table 7: VDD_SPI Voltage Control

VDD_SPI power source [2]	Voltage	EFUSE_VDD_SPI_FORCE	GPIO45	EFUSE_VDD_SPI_TIEH
VDD3P3_RTC via R_{SPI}	3.3 V	0	0	Ignored
Flash Voltage Regulator	1.8 V		1	
Flash Voltage Regulator	1.8 V	1	Ignored	0
VDD3P3_RTC via R_{SPI}	3.3 V			1

[1] Bold marks the default value and configuration.

[2] See *ESP32-S3 Series Datasheet* > Section *Power Scheme*.

43 ROM Messages Printing Control

During boot process the messages by the ROM code can be printed to:

- (Default) UART0 and USB Serial/JTAG controller
- USB Serial/JTAG controller
- UART0

The ROM messages printing to UART or USB Serial/JTAG controller can be respectively disabled by configuring registers and eFuse. For detailed information, please refer to *ESP32-S3 Technical Reference Manual* > Chapter *Chip Boot Control*.

44 JTAG Signal Source Control

The strapping pin GPIO3 can be used to control the source of JTAG signals during the early boot process. This pin does not have any internal pull resistors and the strapping value must be controlled by the external circuit that cannot be in a high impedance state.

As Table 8 shows, GPIO3 is used in combination with EFUSE_DIS_PAD_JTAG, EFUSE_DIS_USB_JTAG, and EFUSE_STRAP_JTAG_SEL.

Table 8: JTAG Signal Source Control

JTAG Signal Source	EFUSE_DIS_PAD_JTAG	EFUSE_DIS_USB_JTAG	EFUSE_STRAP_JTAG_SEL	GPIO3
USB Serial/JTAG Controller	0	0	0	Ignored
	0	0	1	1
	1	0	Ignored	Ignored
JTAG pins [2]	0	0	1	0
	0	1	Ignored	Ignored
JTAG is disabled	1	1	Ignored	Ignored

[1] Bold marks the default value and configuration.

[2] JTAG pins refer to MTDI, MTCK, MTMS, and MTDO.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses above those listed in Table 9 Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Table 10 Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
T_{STORE}	Storage temperature	–40	105	°C

5.2 Recommended Operating Conditions

Table 10: Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
VDD33	Power supply voltage		3.0	3.3	3.6	V
$I_{V\,DD}$	Current delivered by external power supply		0.5	–	–	A
T_A	Operating ambient temperature	65 °C version	–40	–	65	°C
		85 °C version			85	
		105 °C version			105	

5.3 DC Characteristics (3.3 V, 25 °C)

Table 11: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	–	2	–	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	–	VDD[1] + 0.3	V
V_{IL}	Low-level input voltage	–0.3	–	0.25 × VDD[1]	V
I_{IH}	High-level input current	–	–	50	nA
I_{IL}	Low-level input current	–	–	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	–	–	V
V_{OL}[2]	Low-level output voltage	–	–	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1] = 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	–	40	–	mA
I_{OL}	Low-level sink current (VDD[1] = 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	–	28	–	mA
R_{PU}	Internal weak pull-up resistor	–	45	–	kΩ
R_{PD}	Internal weak pull-down resistor	–	45	–	kΩ

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Table 11 – cont'd from previous page

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH_nRST}	Chip reset release voltage (EN voltage is within the specified range)	0.75 × VDD[1]	—	VDD[1] + 0.3	V
V_{IL_nRST}	Chip reset voltage (EN voltage is within the specified range)	–0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for pins of a particular power domain.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

5.4 Current Consumption Characteristics

5.4.1 Current Consumption in Active Mode

With the use of advanced power-management technologies, the module can switch between different power modes. For details on different power modes, please refer to Section *Power Management Unit* in *ESP32-S3 Series Datasheet*.

The current consumption measurements are taken with a 3.3 V supply at 25 °C ambient temperature.

TX current consumption is rated at a 100% duty cycle.

RX current consumption is rated when the peripherals are disabled and the CPU idle.

Table 12: Current Consumption in Avtice Mode

Work mode	Description		Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, @20.5 dBm	355
		802.11g, 54 Mbps, @18 dBm	297
		802.11n, HT20, MCS 7, @17.5 dBm	286
		802.11n, HT40, MCS 7, @17 dBm	285
	RX	802.11b/g/n, HT20	95
		802.11n, HT40	97

Note:
The content below is excerpted from *Section Power Consumption in Other Modes* in *ESP32-S3 Series Datasheet*.

5.4.2 Current Consumption in Other Modes

Please note that if the chip embedded has in-package PSRAM, the current consumption of the module might be higher compared to the measurements below.

Table 13: Current Consumption in Modem-sleep Mode

Work mode	Frequency (MHz)	Description	Typ[1] (mA)	Typ[2] (mA)
Modem-sleep[3]	40	WAITI (Dual core in idle state)	13.2	18.8
		Single core running 32-bit data access instructions, the other core in idle state	16.2	21.8
		Dual core running 32-bit data access instructions	18.7	24.4
		Single core running 128-bit data access instructions, the other core in idle state	19.9	25.4
		Dual core running 128-bit data access instructions	23.0	28.8
	80	WAITI	22.0	36.1
		Single core running 32-bit data access instructions, the other core in idle state	28.4	42.6
		Dual core running 32-bit data access instructions	33.1	47.3
		Single core running 128-bit data access instructions, the other core in idle state	35.1	49.6
		Dual core running 128-bit data access instructions	41.8	56.3
	160	WAITI	27.6	42.3
		Single core running 32-bit data access instructions, the other core in idle state	39.9	54.6
		Dual core running 32-bit data access instructions	49.6	64.1
		Single core running 128-bit data access instructions, the other core in idle state	54.4	69.2
		Dual core running 128-bit data access instructions	66.7	81.1
	240	WAITI	32.9	47.6
		Single core running 32-bit data access instructions, the other core in idle state	51.2	65.9
		Dual core running 32-bit data access instructions	66.2	81.3
		Single core running 128-bit data access instructions, the other core in idle state	72.4	87.9
		Dual core running 128-bit data access instructions	91.7	107.9

[1] Current consumption when all peripheral clocks are disabled.

[2] Current consumption when all peripheral clocks are enabled. In practice, the current consumption might be different depending on which peripherals are enabled.

[3] In Modem-sleep mode, Wi-Fi is clock gated, and the current consumption might be higher when accessing flash. For a flash rated at 80 Mbit/s, in SPI 2-line mode the consumption is 10 mA.

Table 14: Current Consumption in Low-Power Modes

Work mode	Description	Typ (μA)
Light-sleep[1]	VDD_SPI and Wi-Fi are powered down, and all GPIOs are high-impedance.	240
Deep-sleep	RTC memory and RTC peripherals are powered up.	8
	RTC memory is powered up. RTC peripherals are powered down.	7

Power off	CHIP_PU is set to low level. The chip is shut down.	1

[1] In Light-sleep mode, all related SPI pins are pulled up. For chips embedded with PSRAM, please add corresponding PSRAM consumption values, e.g., 140 μA for 8 MB Octal PSRAM (3.3 V), 200 μA for 8 MB Octal PSRAM (1.8 V) and 40 μA for 2 MB Quad PSRAM (3.3 V).

6 Peripheral Schematics

This is the typical application circuit of the module connected with peripheral components (for example, power supply, antenna, reset button, JTAG interface, and UART interface).

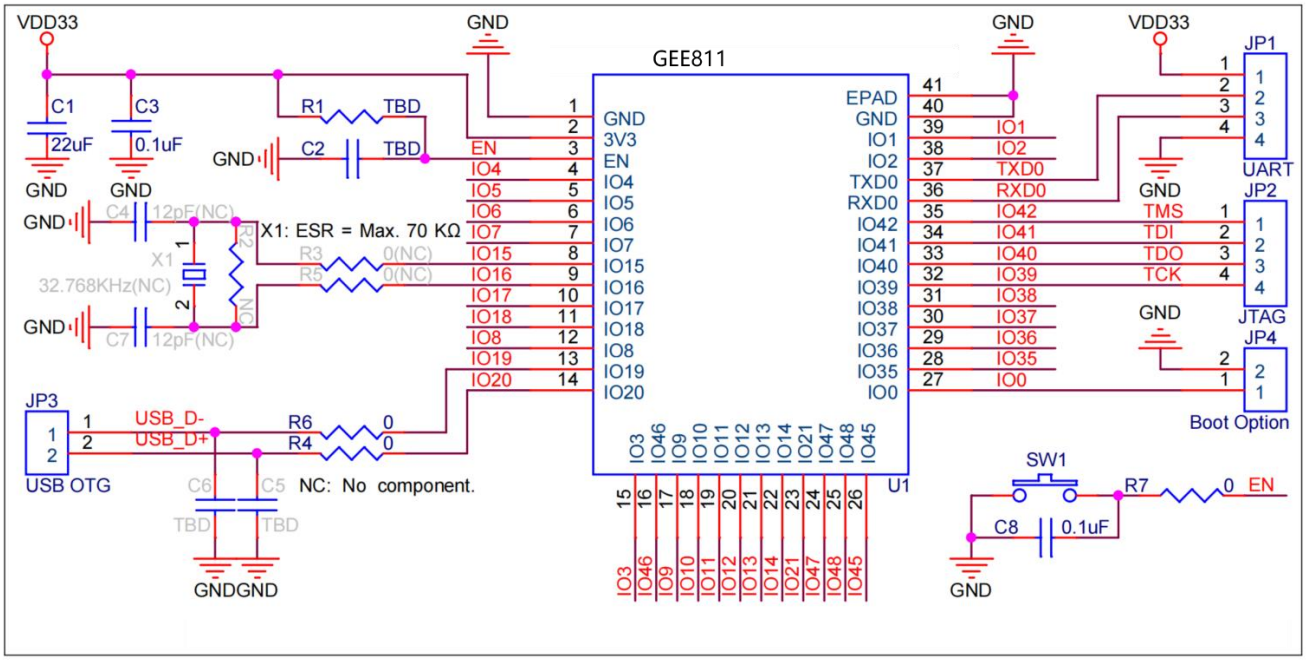

Figure 7: Peripheral Schematics

- Soldering the EPAD to the ground of the base board is not a must, however, it can optimize thermal performance. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32-S3 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S3's power-up and reset sequence timing diagram, please refer to *ESP32-S3 Series Datasheet* > Section *Power Supply*.

7 Physical Dimensions

7.1 Module Dimensions

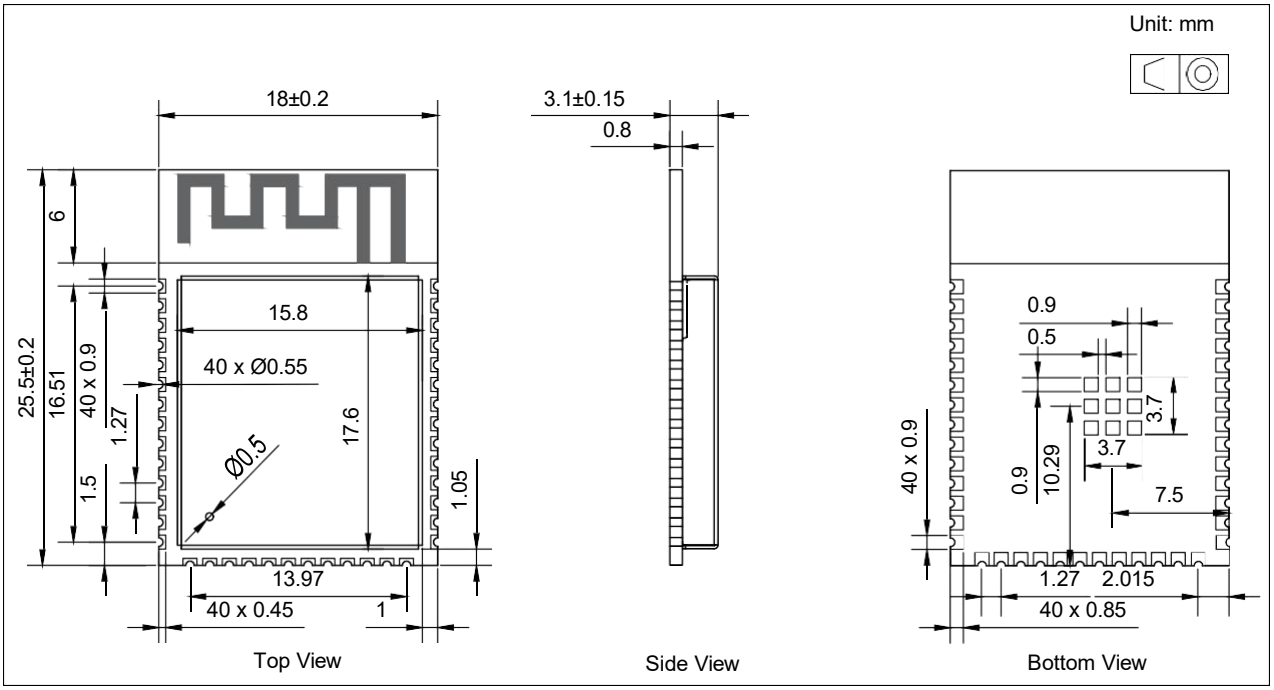

Figure 8: GEE811 Physical Dimensions

8 PCB Layout Recommendations

8.1 PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 11 *GEE811 Recommended PCB Land Pattern*.

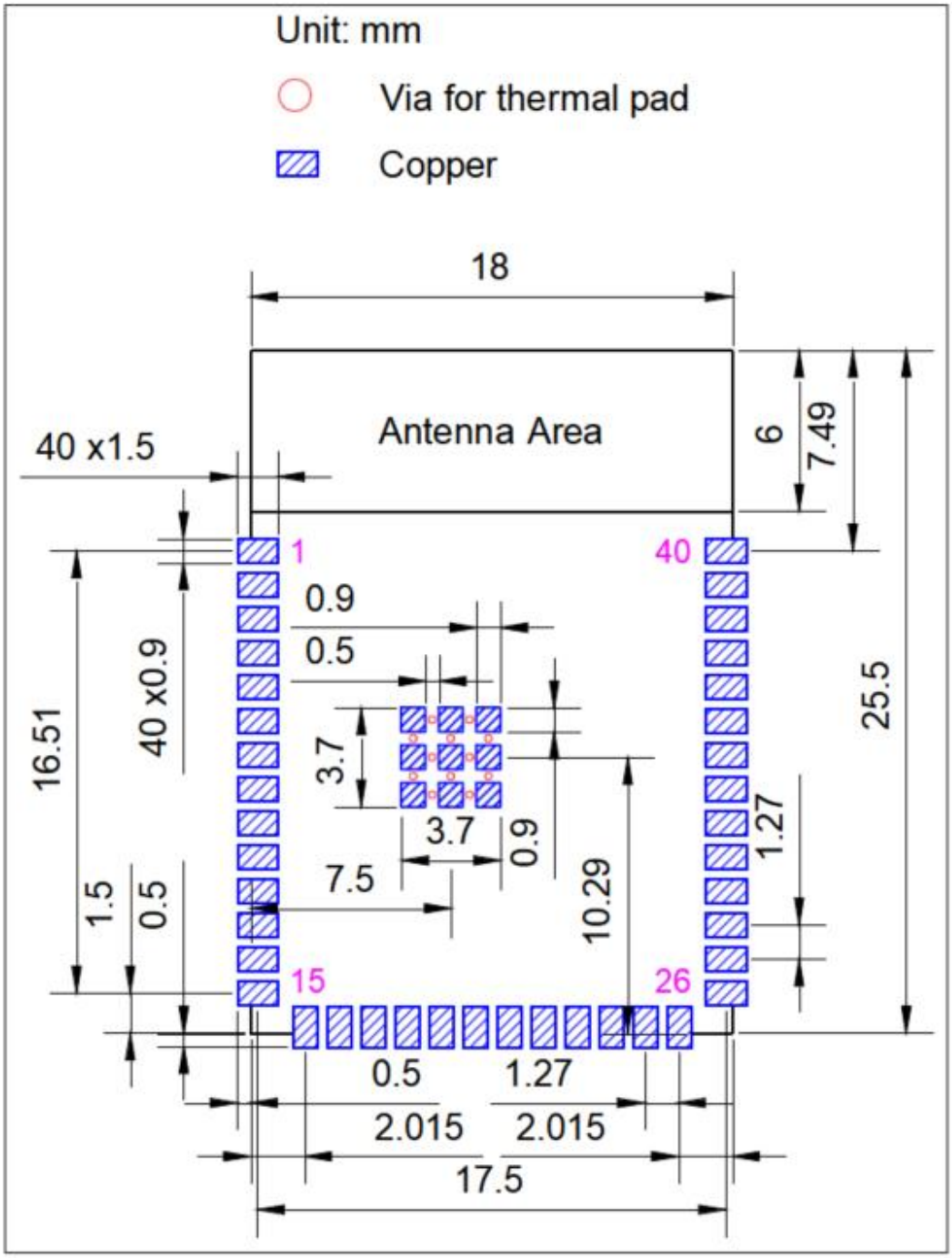

Figure 11: GEE811 Recommended PCB Land Pattern

82 Module Placement for PCB Design

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized. It is suggested to place the module's on-board PCB antenna outside the base board, and the feed point of the antenna closest to the board. In the following example figures, positions with mark ✓ are strongly recommended, while positions without a mark are not recommended.

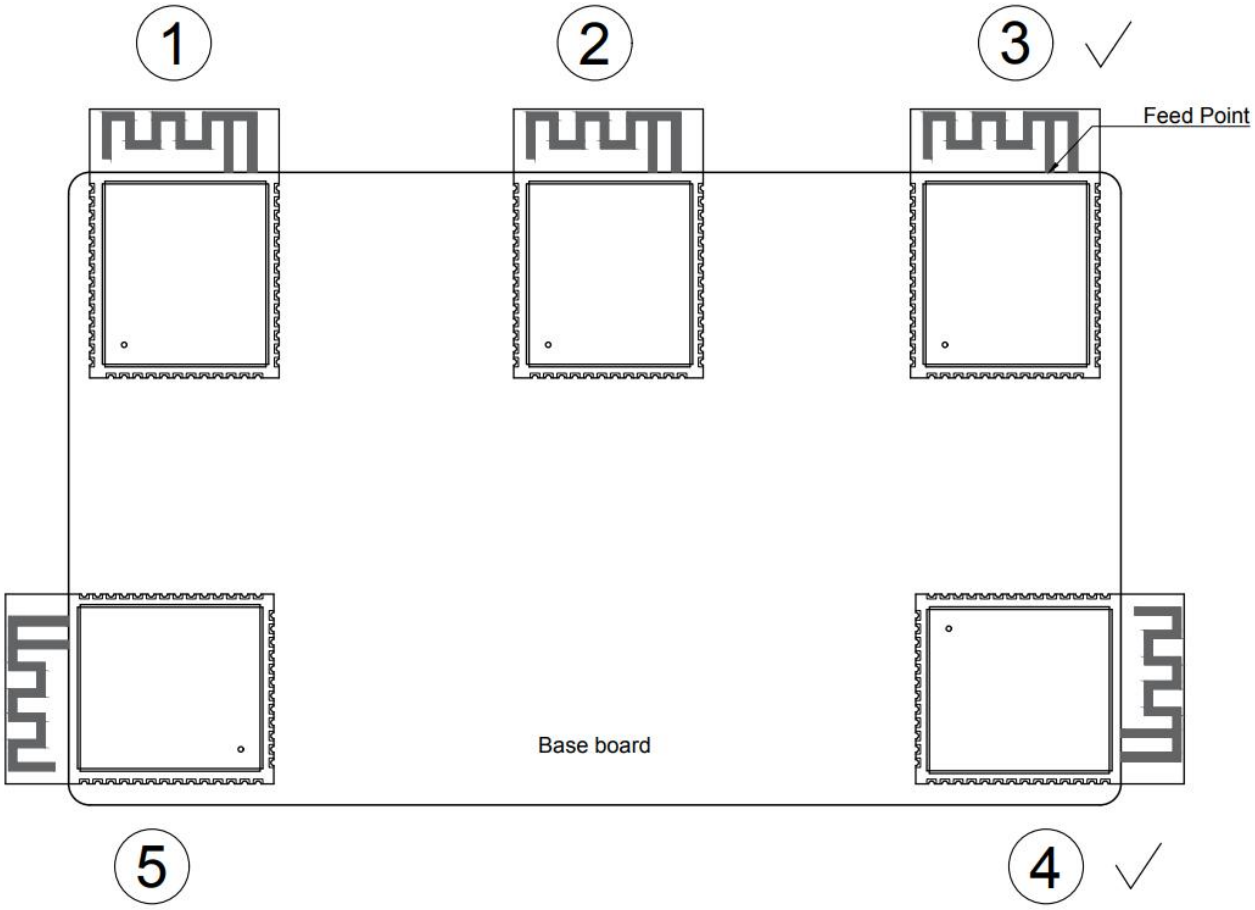

Figure 12: Placement of ESP32-S3 Modules on Base Board (Antenna Feed Point on the Right)

If PCB antenna could not be placed outside the board, please ensure a clearance of at least 15 mm around the antenna area (no copper, routing, or components on it), and place the feed point of the antenna closest to the board. If there is a base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. Figure 16 shows the suggested clearance for modules whose antenna feed point is on the right.

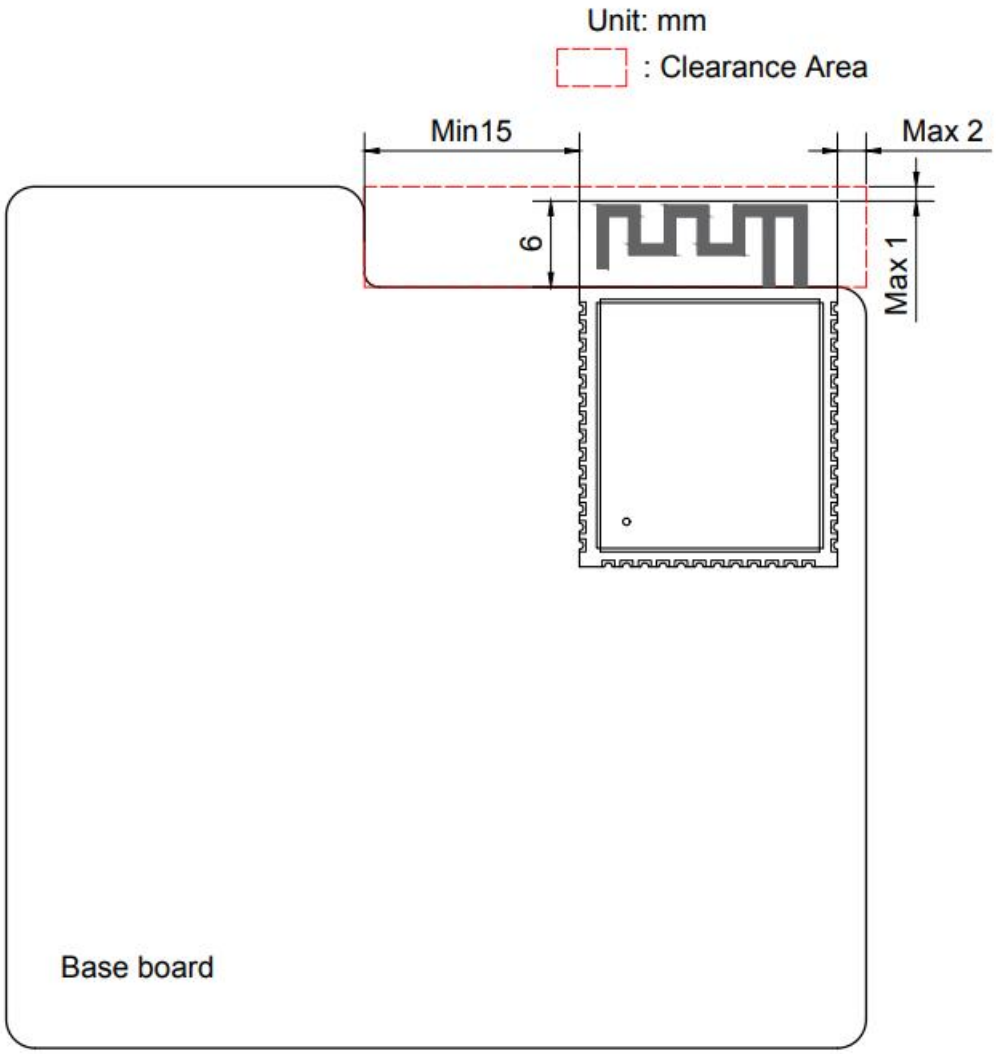

Figure 13: Keepout Zone for ESP32-S3 Module’s Antenna on the Base Board

9 Product Handling

9.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25±5 °C and 60%RH. If the above conditions are not met, the module needs to be baked.

9.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

9.3 Reflow Profile

Solder the module in a single reflow.

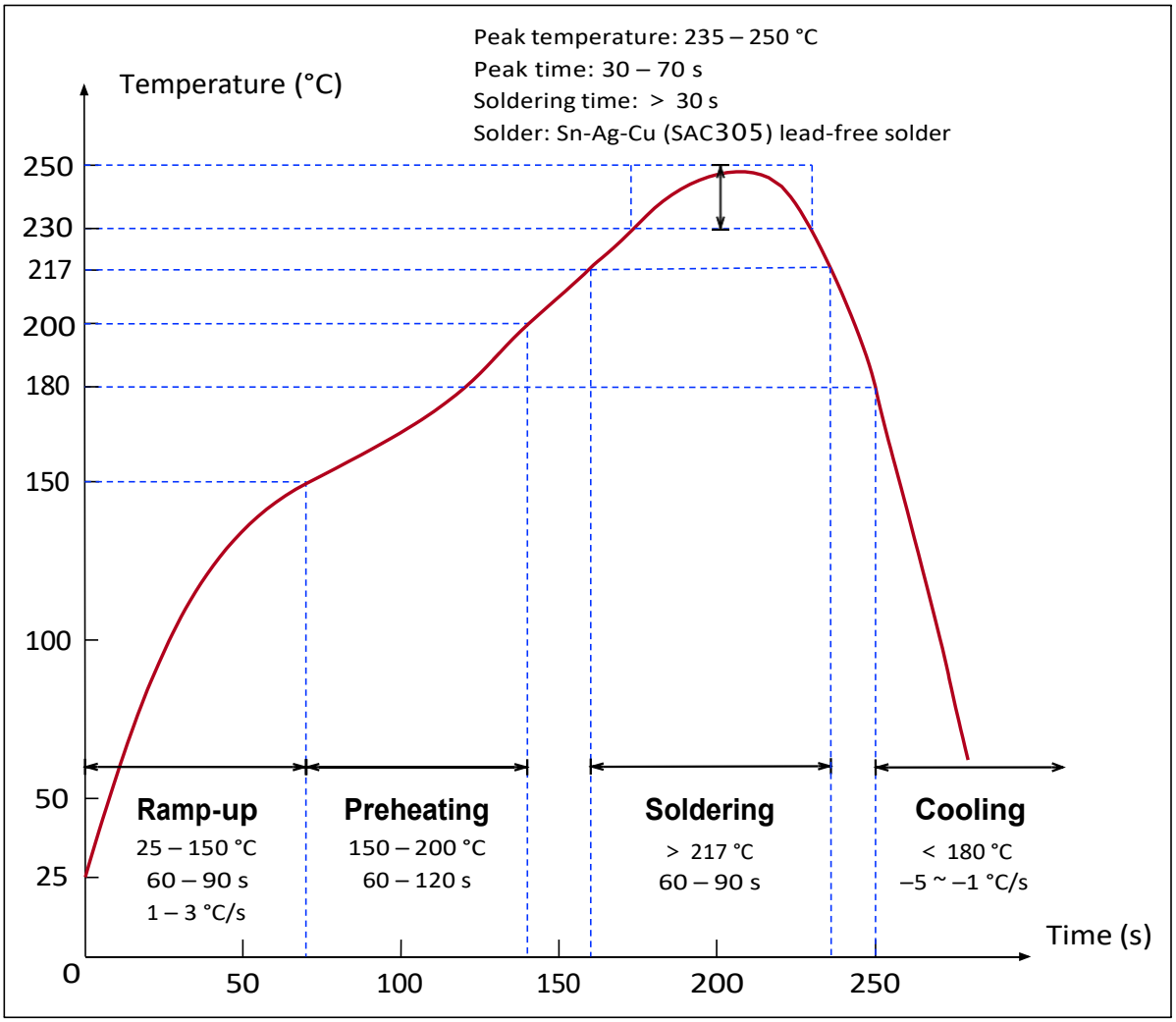

Figure 13: Reflow Profile

9.4 Ultrasonic Vibration

Avoid exposing modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, the module may stop working or its performance may deteriorate.

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This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user' s authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursua nt to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful inte rference in a residential installation. This equipment generates uses and can radiate radio frequency energy a nd, if not installed and used in accordance with the instructions, may cause harmful interference to radio com munications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turn ing the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help important announcement

Important Note:

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Country Code selection feature to be disabled for products marketed to the US/Canada.

This device is intended only for OEM integrators under the following conditions:

1. The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2. The transmitter module may not be co-located with any other transmitter or antenna,
3. For all products market in US, OEM has to limit the operation channels in CH1 to CH11 for 2.4G band by supplied firmware programming tool. OEM shall not supply any tool or info to the end-user regarding to Regulatory Domain change. (if modular only test Channel 1-11)

As long as the three conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Important Note:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The final end product must be labeled in a visible area with the following"

Contains FCC ID: 2ASLM-GEE811 "

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01r01

2.2 List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C has been investigated. It is applicable to the modular transmitter

2.3 Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

2.4 Limited module procedures

Not applicable

2.5 Trace antenna designs

Not applicable

2.6 RF exposure considerations

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

2.7 Antennas

This radio transmitter **FCC ID:**2ASLM-GEE811 has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Antenna No.	Model No. of antenna:	Type of antenna:	Gain of the antenna (Max.)		Frequency range:
			Antenna 1	Antenna 2	
Bluetooth	/	PCB Antenna	0	N/A	2402-2480MHz
2.4G Wi-Fi	/	PCB Antenna	0	N/A	2412-2462MHz

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following" Contains **FCC ID:**2ASLM-GEE811".

2.9 Information on test modes and additional testing requirements

Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

2.10 Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B.

2.11 Note EMI Considerations

Host manufacture is recommended to use D04 Module Integration Guide recommending as "best practice" RF design engineering testing and evaluation in case non-linear interactions generate additional non-compliant limits due to module placement to host components or properties.

2.12 How to make changes

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system. According to the KDB 996369 D02 Q&A Q12, that a host manufacture only needs to do an evaluation (i.e., no C2PC required when no emission exceeds the limit of any individual device (including unintentional radiators) as a composite. The host manufacturer must fix any failure.