Thundersoft TurboX® D820 SOM Datasheet

Thundercomm

Version	Date	Description
V0.1	2018-7-12	Initial Version

Contents

1 Overview

1.1 Abstract

Thundersoft TurboX®D820 is high level performance intelligent module, integrating Android or Linux system, based on Qualcomm APQ8096 processor. It used the advanced 14 nm Fin FET process, customized 64-bit ARMv8-campliant quad-core applications processor, 2.15GHz CPU process performance, integrated a new Adreno 530 graphics processing unit (GPU).

Thundersoft TurboX® D820 support short-range wireless communication through Wi-Fi 802.11 a/b/g/n/ac and BT4.2, and integrates GPS/GLONASS satellite positioning system. Thundersoft TurboX® D820 support 3840*2400@60fps display, it can connect 3 x camera modules, 1080P video smoothly output, and integrating multiple audio and video input/output interfaces. Thundersoft TurboX® D820 provides a variety of GPIO, I2C, UART and SPI standard interfaces. In addition, it supports two MIPI-DSI, three MIPI-CSI and SOM common standard protocol interfaces such as USB3.0, USB2.0, SPI, PCIE2.1, I2S, SLIMBUS and HDMI.

Thundersoft TurboX® D820 provide convenient and stable system software solution for IOT field, it can be embedded into the device on VR/AR, Drone, Robot, Smart Camera, Routers, and any other connecting fields. The size of Thundersoft TurboX® D820 module is 36mm x 51mm x 6.45mm, weight 16g,with 302PINs.

1.2 Reference Documents

Document
80-NT204-1 MSM8996-APQ8096 DEVICE SPECIFICATION
80-NT204-41 MSM8996 BASEBAND REFERENCE SCHEMATIC
80-NJ118-1 PMI8994-PMI8996 POWER MANAGEMENT IC DEVICE SPECIFICATION

1.3 Terms and Acronyms

Acronym/Terminology	Description
ADC	Analog-to-digital converter
BER	Bit error rate

BLSP	BAM-based low-speed peripheral
eMMC	Embedded Multimedia Card
GPIO	General Purpose Input/output
GLONASS	GLONASS Global orbiting navigation satellite system
GNSS	Global navigation satellite system
HDMI	High-Definition Multimedia Interface
LPDDR	Low Power Double Data Rate
LPG	Light Pulse Generators
LCD	Liquid crystal display
MIPI-CSI	Mobile Industry Processor Interface Camera Serial Interface
MIPI-DSI	Mobile Industry Processor Interface Display Serial Interface
MBHC	Multiple button headset control
MOSI	Master output/Slaver input
MISO	Master input/Slaver output
MPP	Multipurpose pin
NFC	Near field communicator
PMIC	Power Management Integrated Circuit
OSC	Oscillator
PA	Power amplifier
PCB	Printed circuit board
PCIe	Peripheral component interconnect express
PCM	Pulse-coded modulation
PM	Power management
PWM	Pulse width modulation
PoP	Package-on-package

SDC	Secure digital controller
SDRAM	Synchronous dynamic random access memory
SLIMbus	Serial Low-power Inter-chip Media Bus
SPI	Serial peripheral interface
SPMI	Serial power management interface
SSC	Snapdragon™ sensor core
TCXO	Temperature-compensated crystal oscillator
SoC	System on Chip
XTAL	Crystal
SDIO	Secure Digital Input / Output
UART	Universal Asynchronous Receiver Transmitter
USB	Universal serial bus
I2S	Inter-IC Sound
I2C	Inter-integrated circuit
WCN	Wireless connectivity network
WLAN	Wireless local area network
SMPS	Switched-mode power supply
SOM	System On Module
ZIF	Zero Insert Force

2 Introduction

2.1 Key features

The following table shows the detailed features and performance on Thundersoft TurboX® D820.

Processors	
Applications Processor	Customized 64-bit ARMv8-compliant quad-core applications processor (Kryo) Two high-performance Kryo cores – gold cluster (2.15 GHz) Two low-power Kryo cores – silver cluster (1.593 GHz)
Digital signal processing	Hexagon DSP with dual-Hexagon vector processor (HVX-512)(target 825 MHz)
Sensor core	Snapdragon™ sensor core (dedicated Q6 low-power island with 512 KB)
Operating System	Android OS 7(TBD)
Memory	64GB UFS+ LPDDR4 4GB Dual-channel PoP high-speed memory – LPDDR4 SDRAM designed for 1866 MHz clock.
Multimedia	
Display support	2 x 4-lane DSI DPHY 1.2 and HDMI 2.0 (4K60) or 4K30 Miracast HDMI up to 3840 x 2160 at 60fps Maximum concurrency configurations 3840x2400 or 4096x2160 at 60Hz primary + 3840x2160 or 4096x2160 at 60Hz HDMI

	2560x1600 at 60 fps primary + 2560x1600 at 60fps secondary + 3840x2160 at 60fps HDMI
Camera support	Support 3 x 4-lane MIPI_CSI Dual 14-bit ISP 28 MP + 13 MP, 600 MHz each 32MP 30ZSL with dual-ISP 16 MP30 ZSL with single ISP ABF3 with radius noise reduction, Demosaic4, TNR, ASF2.2, Dual AF, LTM, CAC2, GIC, Pedestal correction, stats upgrades
Video	
Encode	H.264 BP/MP/HP, MPEG-4 SP/ASP, H.263 P0, VP8, HEVC Main Maximum performance 3840x2160 at 30 fps 4096x2160 at 24 fps
Decode	H.264 BP/MP/HP, MPEG-4 SP/ASP, H.263 P0, VC1 SP/MP/AP, MPEG-2 MP, DivX 3.11/4/5/6, VP8, VP9, HEVC Main, HEVCMain10* Maximum performance 3840x2160 at 60 fps 4096x2160at 60 fps
Graphics	Adreno 530 3D graphics accelerator 624 MHz Support by A530 for all important GPU APIs DirectX 12 _FL12 (future-proof DX)

	OpenGL ES 3.1*+AEP1 and Vulkan OpenCL 2.0*(full), RenderScript Support for 64-bit virtual addresses, allowing for SVM with 64-bit CPUs Supports GPU virtualization
Audio*(build in Thundersoft TurboX® D820 Carrier Board with WCD9335 codec)*	
Codec	Seven DACs, seven outputs Six differential analog inputs with dedicated ADCs Six digital microphones Snapdragon™ voice activation (SVA) subsystem for ultra low voice wake-up MBHC, ANC 130 dB dynamic range, 24-bit DAC 44.1 kHz native playback SLIMbus to I2S bridge
Low-power audio	Low-power, low-complexity; 7.1 surround sound
Voice codec support	QCELP, EVRC, EVRC-B, EVRC-WB,EVS, GSM-FR, -EFR, -HR; AMR-NB, -WB
Audio Encoders	QCELP, EVRC, AMR-WB, AMR-NB, AAC ELD, AAC and AAC+
Audio Decoders	PCM playback, AAC/AAC+/eAAC+, MP3, WMA (v9 and v10), WMALossless, WMAPro10, AMR-NB, AMR-WB, AMR-WB+, FLAC, ALAC, Vorbis*, AIFF, APE, AC3, eAC3, M8
Enhanced audio	Surround sound: DTS-HD; DTS express 7.1 Fluence noise cancellation; enhanced speaker protection

	QAudioFX/Qconcert/QEnsemble
Wireless connectivity	
WLAN	2.4G/5G, support 802.11 a/b/g/n/ac, 2 X 2 MIMO Support AP mode
Bluetooth	Support Bluetooth 4.2 + HS BLE, Backwards compatible with Bluetooth 1.2, 2.X + enhanced data rate.
GNSS	Support GPS/GLONASS
Connectivity	
USB	Two – one USB 2.0 high-speed and one USB 3.0 super-speed/USB 2.0 high-speed Compliant
HDMI	Integrated HDMI Tx core and HDMI PHY Rev 2.0 1080p at 60 Hz refresh; 24-bit RGB color 4k 60 fps HDMI 2-channel Linear Pulse-Code Modulation (LPCM) 8-channel LPCM 24 bit/192 kHz
PCIe	2x PCIe, PCIe v2.1 PHY and 2.1 controller
SDIO	1 x 4-bit, SD 3.0 SD/MMC card, eMMC NAND, eSD/eMMC boot
BLSP	7 BLSPs ,can be configured as SPI or I2C or UART

UART	up to 4 MHz
I2C	Sensors etc
SPI	Sensors etc
SLIMbus	One, highly multiplexed, high-speed, baseline WCD9335
MI2S	3 ports; Full duplex stereo or up to quad channel Tx/Rx MI2S (x1); Up to 2 channel for multi-channel audio applications (x2);
PCM	Short and long sync PCM support
GPIO	6+ GPIO ports
Others	
ADC Interface	Support ADC interfaces used for input voltage sense, battery temperature detection and general purpose ADC
Touch screen support	Capacitive panels via ext IC (I2C, SPI, and interrupts)
Physical size	Size: 36mm x 51mm x 6.45mm Weight: approx.16g Interface: Connector
Operating temperature	-10C ~55C

RoHS	All hardware components are fully compliant with EU RoHS directive

Table 2.1-1Detailed features and performance

2.2 Major Components Location

Thundersoft TurboX® D820 SOM's major components are as below.

There are another 2 pieces shielding covers which will be covered at the top and bottom shielding frame.

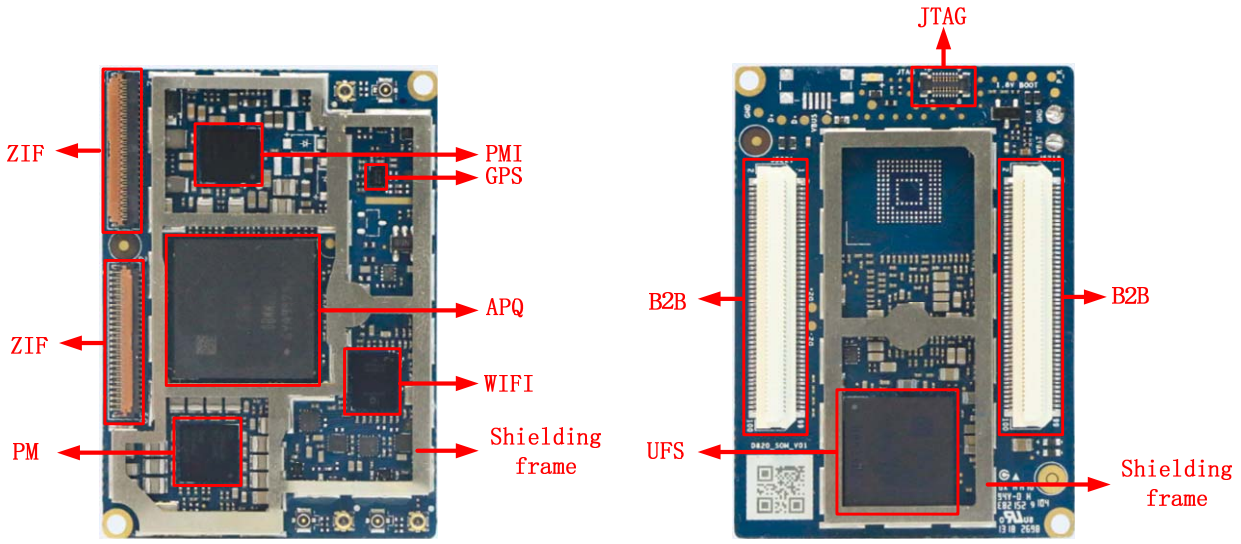

Figure 2.2-1ThundersoftTurboX® D820 SoM Key component Location

2.3 Connectors Function and Part Number

We have SOM major parts connectors on Thundersoft TurboX® D820. Below map can easy to show the Pin start & end location on connector.

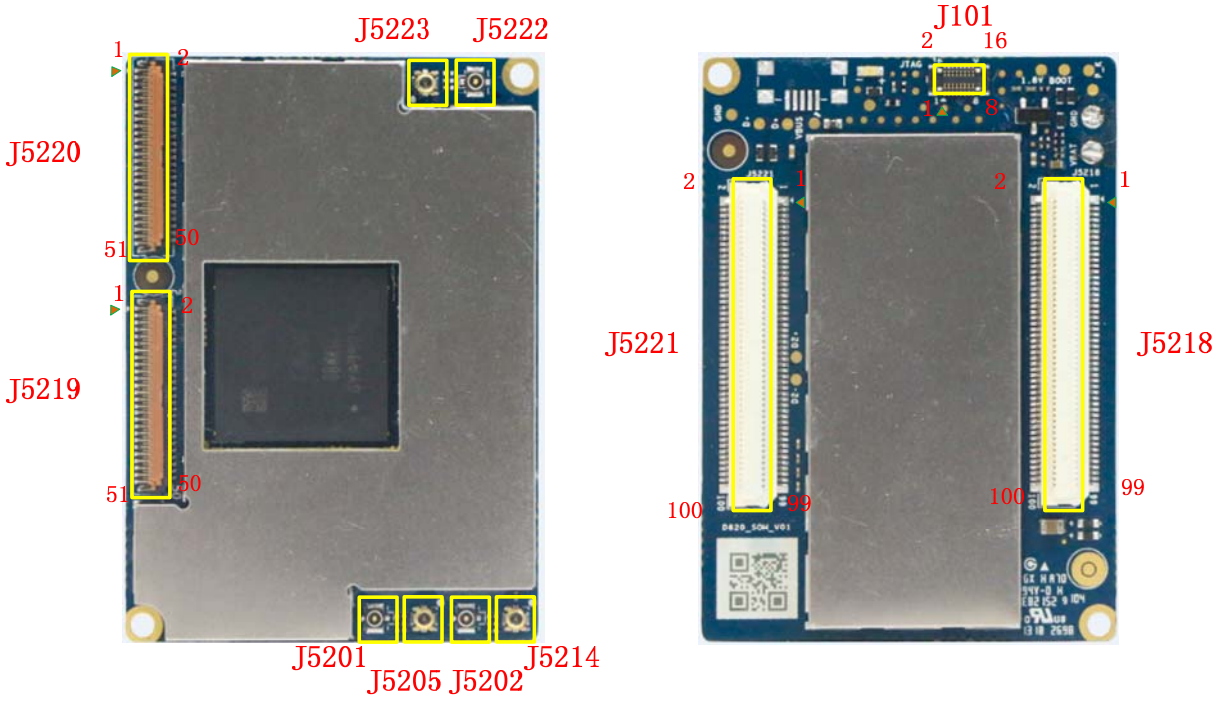

Figure 2.3-1ThundersoftTurboX® D820 SOM Connector PIN Location

Thundersoft TurboX® D820 SOM Below table indicates connectors detail information.

Part Reference	Description	Manufacturer Part Number	Manufacturer
J5218,J5221	BTB connectors, used for connecting to Carrier Board.	AXK6S00437YG	PANASONIC
J5219,J5220	ZIF connectors, used for extended CSI/DSI/SENSOR/GPIOs	FH26W-51S-0.3SHW(05)	HIROSE
J5201,J5202	J5201 is an antenna connector for Wi-Fi/BT; J5202 is an antenna connector for Wi-Fi.	818000157	ECT
J5222	An antenna connector for GPS;	818000157	ECT
J5205,J5214	Wifi/bt calibration and test socket	MM8030-2610RK0	MURATA
J5223	GPS test socket	MM8030-2610RK0	MURATA
J101	JTAG connector	AXG7160J7	PANASONIC

Table 2.3-1Connector part number and information

3 Interfaces Description

This chapter introduces all the interfaces definition, purpose to guide developer easy to design and verification on Thundersoft TurboX® D820 SOM.

3.1 Interfaces Parameter Definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
CSI	Supply voltage for MIPI_CSI circuits and I/O; (1.8 V only)
DI	Digital input(CMOS)
DSI	Supply voltage for MIPI_DSI I/O; (1.8 V only)
DO	Digital output(CMOS)
H	High-voltage tolerant
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain
PD	Contains an internal pull-down device

PI	Power input
PO	Power output
PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
P3	Power group 3,it is 1.8V.
P2	SDC Power group 3,it is 1.8V or 2.95V.
P12	SSC Power group 12,it is 1.8V.

Table 3.1-1Interfaces parameter definitions

3.2 Interfaces Detail Description

3.2.1 Power Supply Interface

Below table describes all interfaces of SOM Power Supply. For the detail parameter request, please refer the chapter on Electrical specifications.

Power Supply					
PIN Name	**Location**	**PIN**	**Type**	**Description**	**Notes**
VBATT	J5218	1,3,5,7,9,11	PI	Power supply in for SOM all operations.	
VBUS_USB_IN	J5218	2,4	PI,PO	USB input power sources or output during USB-OTG operation.	
VREG_S4A_1P8	J5218	8	PO	Used for 1.8V IO pull up voltage;	
VREG_L21A_2P95	J5218	18	PO	Power output for SD card	
VCOIN	J5218	46	AI,AO	Coin cell battery or backup battery;	
GND	J5218	10,16,22,28,27,29,31,33,34,40,43,47,	GND		
	J5221	1,2,5,8,9,13,14,20,25,26,31,32,37,38,43,44,49,50,55,5	GND		

		6,61,62,67,68,73,74,79,85,88,91,97			
	J5219	6,12,14,16	GND		
	J5220	1,4,7,10,13,16,18,25,36,39,42,45,48,51	GND		

Table 3.2-1 Power Supply Definition

3.2.2 Touch screen Interface

Touch screen panels are supported using I2C buses and GPIOs configured as discrete digital inputs.

Touch screen						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
BLSP12_GPIO_87	J5218	60	P3	OD	BLSP12 I2C signals sda	
BLSP12_GPIO_88	J5218	58	P3	OD	BLSP12 I2C signals scl	
BLSP12_GPIO_85	J5218	64	P3	DO	BLSP12 UART signals tx	TP-RST
BLSP12_GPIO_86	J5218	62	P3	DI	BLSP12 UART signals rx	TP-INT

Table 3.2-2Touchscreen interfaces definition

3.2.3 Display Interface

The SOM supports dual 4-lane MIPI_DSI interfaces.

Display						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
MIPI_DSI0_CLK_P_CON	J5218	12	DSI	AO	MIPI0 signals for MIPI LCM. Compliant with MIPI Alliance Specification for Display Serial Interface	
MIPI_DSI0_CLK_N_CON	J5218	14	DSI	AO		
MIPI_DSI0_LANE3_P_CON	J5218	18	DSI	AO		
MIPI_DSI0_LANE3_N_CON	J5218	20	DSI	AO		
MIPI_DSI0_LANE2_P_CON	J5218	24	DSI	AO		
MIPI_DSI0_LANE2_N_CON	J5218	26	DSI	AO		
MIPI_DSI0_LANE0_P_CON	J5218	30	DSI	AO		
MIPI_DSI0_LANE0_N_CON	J5218	32	DSI	AO		
MIPI_DSI0_LANE1_P_CON	J5218	36	DSI	AO		
MIPI_DSI0_LANE1_N_CON	J5218	38	DSI	AO		

MIPI_DSI1_LANE3_N_CON	J5220	37	DSI	AO	MIPI1 Signals for MIPI LCM Compliant with MIPI Alliance Specification for Display Serial Interface	
MIPI_DSI1_LANE3_P_CON	J5220	38	DSI	AO		
MIPI_DSI1_LANE0_N_CON	J5220	40	DSI	AO		
MIPI_DSI1_LANE0_P_CON	J5220	41	DSI	AO		
MIPI_DSI1_LANE2_N_CON	J5220	43	DSI	AO		
MIPI_DSI1_LANE2_P_CON	J5220	44	DSI	AO		
MIPI_DSI1_CLK_N_CON	J5220	46	DSI	AO		
MIPI_DSI1_CLK_P_CON	J5220	47	DSI	AO		
MIPI_DSI1_LANE1_N_CON	J5220	49	DSI	AO		
MIPI_DSI1_LANE1_P_CON	J5220	50	DSI	AO		

Table 3.2-3Display interfaces definition

3.2.4 Camera Interfaces

The SOM supports 3x 4-lane camera interfaces.CSI0 and CSI1 connection are from B2B connector J5221, CSI2 is from zif connector J5220. There are only 2 I2C interfaces for three CSI, so it needs pay attention to the camera module I2C address.

Camera1 Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
CAM_MCLK0	J5221	3	P3	DO	Camera0 main clock output	
MIPI_CSI0_CLK_N	J5221	28	CSI	AI	MIPI Signals of Camera0 Compliant with MIPI Alliance Standard Specification	
MIPI_CSI0_CLK_P	J5221	30	CSI	AI		
MIPI_CSI0_LANE0_N	J5221	34	CSI	AI		
MIPI_CSI0_LANE0_P	J5221	36	CSI	AI		
MIPI_CSI0_LANE1_N	J5221	40	CSI	AI		
MIPI_CSI0_LANE1_P	J5221	42	CSI	AI		
MIPI_CSI0_LANE2_N	J5221	46	CSI	AI		
MIPI_CSI0_LANE2_P	J5221	48	CSI	AI		
MIPI_CSI0_LANE3_N	J5221	52	CSI	AI		
MIPI_CSI0_LANE3_P	J5221	54	CSI	AI		
Camera2 Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
CAM_MCLK1	J5221	7	P3	DO	Camera1 main clock output	
MIPI_CSI1_CLK_N	J5221	27	CSI	AI	MIPI Signals of	

MIPI_CSI1_CLK_P	J5221	29	CSI	AI	Camera1 Compliant with MIPI Alliance Standard Specification	
MIPI_CSI1_LANE0_N	J5221	33	CSI	AI		
MIPI_CSI1_LANE0_P	J5221	35	CSI	AI		
MIPI_CSI1_LANE1_N	J5221	39	CSI	AI		
MIPI_CSI1_LANE1_P	J5221	41	CSI	AI		
MIPI_CSI1_LANE2_N	J5221	45	CSI	AI		
MIPI_CSI1_LANE2_P	J5221	47	CSI	AI		
MIPI_CSI1_LANE3_N	J5221	51	CSI	AI		
MIPI_CSI1_LANE3_P	J5221	53	CSI	AI		

Camera3 Interface

PIN Name	Location	PIN	Voltage	Type	Description	Notes
CAM_MCLK2	J5221	11	P3	DO	Camera2 main clock output	
MIPI_CSI2_LANE3_P	J5220	2	CSI	AI	MIPI Signals of Camera2 Compliant with MIPI Alliance Standard Specification	
MIPI_CSI2_LANE3_N	J5220	3	CSI	AI		
MIPI_CSI2_LANE2_P	J5220	5	CSI	AI		
MIPI_CSI2_LANE2_N	J5220	6	CSI	AI		
MIPI_CSI2_LANE0_P	J5220	8	CSI	AI		
MIPI_CSI2_LANE0_N	J5220	9	CSI	AI		
MIPI_CSI2_LANE1_P	J5220	11	CSI	AI		
MIPI_CSI2_LANE1_N	J5220	12	CSI	AI		
MIPI_CSI2_CLK_P	J5220	14	CSI	AI		
MIPI_CSI2_CLK_N	J5220	15	CSI	AI		

Camera I2C Interface

CCI_I2C_SDA0	J5221	15	P3	OD	CCI0 Date signal, already pull up on SOM with 2.2k resistor	
CCI_I2C_SCL0	J5221	17	P3	OD	CCI0 Clock signal, already pull up on SOM with 2.2k resistor	
CCI_I2C_SDA1	J5221	19	P3	OD	CCI1 Date signal, already pull up on SOM with 2.2k resistor	
CCI_I2C_SCL1	J5221	21	P3	OD	CCI1 Clock signal, already pull up on SOM with 2.2k resistor	

Table 3.2-4Camera interface definition

3.2.5 Audio Interface

The SOM provide SLIMBUS, I2S interfaces and PCM interface for audio. SLIMBUS interface is dedicate for external codec IC(wcd9335), which can build system's audio functions. I2S and PCM share the same interfaces which can connect audio devices.

PIN Name	Location	PIN	Voltage	Type	Description	Notes
SlimBus Interface						
PM_GPIO_15	J5218	45	1.8V	DO	External codec clk	
GPIO_71	J5218	37	P3	IO	SLIMBUS_DATA0	Slimbus, connect to COEDC, Compliant with MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01
GPIO_72	J5218	35	P3	IO	SLIMBUS_DATA1	
GPIO_70	J5218	39	P3	DO	SLIMBUS_CLK	
GPIO_64	J5218	49	P3	DO	CODEC reset output	
BLSP7_GPIO_54	J5218	63	P3	DI	CODEC interrupt 1input	
BLSP7_GPIO_53	J5218	65	P3	DI	CODEC interrupt 2input	
I2S2(PCM2) Interface						
GPIO_79	J5218	90	P3	DO	I2S_2_MCLK	
GPIO_80	J5218	88	P3	DO	I2S_2_SCK/PCM2_CLK	
BLSP5_GPIO_81	J5218	86	P3	DO	I2S_2_WS/PCM2_SYNC	
BLSP5_GPIO_82	J5218	84	P3	DI/DO	I2S_2_D0/PCM2_DIN	
BLSP5_GPIO_83	J5218	82	P3	DI/DO	I2S_2_D1/PCM2_DOUT	
I2S3(PCM3) Interface						
GPIO_74	J5218	100	P3	DO	I2S_3_MCLK	
GPIO_75	J5218	98	P3	DO	I2S_3_SCK/PCM3_CLK	
GPIO_76	J5218	96	P3	DO	I2S_3_WS/PCM3_SYNC	
GPIO_77	J5218	94	P3	DI/DO	I2S_3_D0/PCM3_DIN	
GPIO_78	J5218	92	P3	DI/DO	I2S_3_D1/PCM3_DOUT	
I2S4(PCM4) Interface						
GPIO_57_FORCE_USB_BOOT	J5218	78	P3	DO	I2S_4_MCLK	The default setting is for usb boot gpio

BLSP11_GPIO_58	J5218	76	P3	DO	I2S_4_SCK/PCM4_CLK	
BLSP11_GPIO_59	J5218	74	P3	DO	I2S_4_WS/PCM4_SYNC	
BLSP11_GPIO_60	J5218	72	P3	DI/DO	I2S_4_D0/PCM4_DIN	
BLSP11_GPIO_61	J5218	70	P3	DI/DO	I2S_4_D1/PCM4_DOUT	
GPIO_62	J5218	68	P3	DI/DO	I2S_4_D2	
GPIO_63	J5218	66	P3	DI/DO	I2S_4_D3	

Table 3.2-5Audio interface definition

3.2.6 USB Interface

The SOM support USB host and slave. Dual USB port support, one is USB 2.0 high-speed for host, the other is USB 3.0 super-speed/USB 2.0 high-speed compliant

SS/HS USB (3.0/2.0) Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
USB3_SS_RX0_P	J5221	58		AI	USB 3.0 Signals Compliant with USB 3.0 standard specification	Require differential impedance of 90Ω.
USB3_SS_RX0_M	J5221	60		AI		
USB3_SS_TX0_P	J5221	64		AO		
USB3_SS_TX0_M	J5221	66		AO		
USB3_HS_D_P	J5221	70		AI,AO	USB 2.0 Signals Compliant with USB 2.0 standard specification	Require differential impedance of 90Ω.
USB3_HS_D_M	J5221	72		AI,AO		
VBUS_USB_IN	J5218	2,4		PI	USB VBUS input	
USB3_HS_USB_ID	J5218	6		AI	USB 2.0 for ID input	
BLSP3_GPIO_47	J5220	24	P3	DO	Type C USB SS switch GPIO	Could be changed based on software configure
HS USB (2.0) Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
USB2_HS_D_P	J5221	57		AI,AO	USB 2.0 Signals Compliant with USB 2.0 standard specification	Require differential impedance of 90Ω.
USB2_HS_D_M	J5221	59		AI,AO		
VBUS_USB_IN	J5218	2,4		PI	USB VBUS input	

Table 3.2-6USB interface definition

3.2.7 HDMI Interface

The SOM supports one HDMI2.0 output interface. Complete 4K 60fps entertainment system, also supports the audio portion of HDMI using internal CPU audio setting.

HDMI Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
GPIO_31	J5218	54	P3	IO	HDMI_CEC	
GPIO_32	J5218	52	P3	OD	HDMI_DDC_CLK	
GPIO_33	J5218	50	P3	OD	HDMI_DDC_DATA	
GPIO_34	J5218	48	P3	DI	HDMI_HPD_CON	
MSM_HDMI_TX0_P	J5221	4		AO	HDMI_TX0_P	
MSM_HDMI_TX0_M	J5221	6		AO	HDMI_TX0_M	
MSM_HDMI_TCLK_P	J5221	10		AO	HDMI_TCLK_P	
MSM_HDMI_TCLK_M	J5221	12		AO	HDMI_TCLK_M	
MSM_HDMI_TX2_P	J5221	16		AO	HDMI_TX2_P	
MSM_HDMI_TX2_M	J5221	18		AO	HDMI_TX2_M	
MSM_HDMI_TX1_P	J5221	22		AO	HDMI_TX1_P	
MSM_HDMI_TX1_M	J5221	24		AO	HDMI_TX1_M	

Table 3.2-7HDMI interface definition

3.2.8 PCIe Interface

The SOM supports two Peripheral Component Interconnect Express (PCIe) interfaces, which can be used for general-purpose peripherals.

PCIE1 Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PCIE1_REFCLK_N	J5221	63		AO	PCIe Signals Compliant with PCI Express Specification Revision 2.1	
PCIE1_REFCLK_P	J5221	65		AO		
PCIE1_MSM_RX_N	J5221	69		AI		
PCIE1_MSM_RX_P	J5221	71		AI		
PCIE1_MSM_TX_N	J5221	75		AO		
PCIE1_MSM_TX_P	J5221	77		AO		
GPIO_130	J5221	29	P3	DO	PCIe reset signal	PCIE1_RST_N
GPIO_131	J5221	35	P3	DI	PCIe clock require signal, need to reserve pull up	PCIE1_CLKREQ_N

					resistor	
GPIO_132	J5221	37	P3	DI	PCIe wake up signal	PCIE1_WAKEUP
PCIE2 Interface						
PCIE2_REFCLK_N	J5221	81		AO	PCIe Signals Compliant with PCI Express Specification Revision 2.1	
PCIE2_REFCLK_P	J5221	83		AO		
PCIE2_MSM_RX_N	J5221	87		AI		
PCIE2_MSM_RX_P	J5221	89		AI		
PCIE2_MSM_TX_N	J5221	93		AO		
PCIE2_MSM_TX_P	J5221	95		AO		
GPIO_114	J5221	82	P3	DO	PCIe reset signal	PCIE2_RST_N
GPIO_115	J5221	84	P3	DI	PCIe clock require signal, need to reserve pull up resistor	PCIE2_CLKREQ_N
GPIO_116	J5221	86	P3	DI	PCIe wake up signal	PCIE2_WAKEUP

Table 3.2-8PCIe interface definition

3.2.9 SSC Interface

The SOM has an integrated sensor subsystem called Snapdragon™ sensor core (SSC), which is dedicated to support low-power, always-on use cases.

The sensor subsystem can be left powered on even when the rest of the device is in sleep mode. The SSC has a dedicated 512 kB L2 cache.

The SSC core has dedicated I/O to communicate with the sensors. The I/O scan support I2C and SPI interfaces.

SSC Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
SPI_CS_N_MAG	J5219	38	P12	DO	SSC SPI1 chip select 2	
SSC_PWR_EN	J5219	39	P12	DO	SSC power enable output	
SSC_I2C_3_SDA	J5219	40	P12	OD/OI	SSC I2C3 serial data	
SSC_I2C_3_SCL	J5219	41	P12	OD	SSC I2C3 serial clock	
SSC_I2C_2_SDA	J5219	42	P12	OD/OI	SSC I2C2 serial data	
SSC_I2C_2_SCL	J5219	43	P12	OD	SSC I2C2 serial clock	
SSC_SPI_1_CS_N	J5219	44	P12	DO	SSC SPI1 chip select 1	
SSC_SPI_1_CLK	J5219	45	P12	DO	SSC SPI1 serial clock	
SSC_SPI_1_MOSI	J5219	46	P12	DO	SSC SPI1 data master out /slaver in	
SSC_SPI_1_MISO	J5219	47	P12	DI	SSC SPI1 data master in /slaver out	

SSC_SPI_3_CLK	J5219	48	P12	DO	SSC SPI3 chip select 1	
SSC_SPI_3_CS_N	J5219	49	P12	DO	SSC SPI3 serial clock	
SSC_SPI_3_MOSI	J5219	50	P12	DO	SSC SPI3 data master out /slaver in	
SSC_SPI_3_MISO	J5219	51	P12	DI	SSC SPI3 data master in /slaver out	

Table 3.2-9SSC interface definition

3.2.10 SDIO Interface

The SOM supports 4-laneSDIO for SD-card.
The SDIO is high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF and so on).

- The clock can be up to 200 Mhz.
- The signals routing should be 50ohm±10% impedance control.
- CLK to DATA/CMD length matching less than 1mm.
- The spacing to all other signals should 2X line width
- Maximum bus capacitance less than 1.0pF.
- Each trace needs to be next to a ground plane.

SDIO (SDC2) Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
SDC2_SDCARD_D3	J5221	90	P2	IO		
SDC2_SDCARD_CMD	J5221	92	P2	DO		
SDC2_SDCARD_CLK	J5221	94	P2	DO		
SDC2_SDCARD_D0	J5221	96	P2	IO		
SDC2_SDCARD_D1	J5221	98	P2	IO		
SDC2_SDCARD_D2	J5221	100	P2	IO		
GPIO_79	J5218	90	P3	DI	SD_CARD_DET_N	Could be changed to other interrupt GPIO

Table 3.2-4SDIO interface definition

3.2.11 BLSP Interface

These GPIOs are available as BAM-based low-speed peripheral (BLSP) interface ports that can be configured for UART, SPI, or I2C operation.
The UART is based on cpu direction.

I2C is a two-wire bus that can be routed to multiple devices; there are no pull-up resistors on SOM board for I2C bus; so if it is configured as I2C interface by software, it needs to pull up to IO voltage with resistors on IO board.

PIN Name	Location	PIN	Voltage	Type	Description	Notes
BLSP1 Interface						
BLSP1_GPIO_0	J5219	22	P3	DO	spi_mosi/uart_tx	
BLSP1_GPIO_1	J5219	23	P3	DI	spi_miso/uart_rx	
BLSP1_GPIO_2	J5219	24	P3	DODI/ODOI	spi_cs/uart_cts/i2c_sda	
BLSP1_GPIO_3	J5219	25	P3	DO/ODOI	spi_clk/uart_rfr/i2c_scl	
GPIO_23	J5218	91	P3	DO	spi_cs3	
GPIO_24	J5218	89	P3	DO	spi_cs2	
GPIO_90	J5220	32	P3	DO	spi_cs1	
BLSP3 Interface						
BLSP3_GPIO_47	J5220	24	P3	ODOI	i2c_sda	
BLSP3_GPIO_48	J5220	23	P3	OD	i2c_scl	
BLSP5 Interface						
BLSP5_GPIO_81	J5218	86	P3	DO	spi_mosi/uart_tx	
BLSP5_GPIO_82	J5218	84	P3	DI	spi_miso/uart_rx	
BLSP5_GPIO_83	J5218	82	P3	DODI/ODOI	spi_cs/uart_cts/i2c_sda	
BLSP5_GPIO_84	J5218	80	P3	DO/ODOI	spi_clk/uart_rfr/i2c_scl	
BLSP6 Interface						
BLSP6_GPIO_25	J5218	99	P3	DO	spi_mosi/uart_tx	
BLSP6_GPIO_26	J5218	97	P3	DI	spi_miso/uart_rx	
BLSP6_GPIO_27	J5218	95	P3	DODI/ODOI	spi_cs/uart_cts/i2c_sda	
BLSP6_GPIO_28	J5218	93	P3	DO/ODOI	spi_clk/uart_rfr/i2c_scl	
BLSP7 Interface						
BLSP7_GPIO_53	J5218	65	P3	DO	spi_mosi/uart_tx	
BLSP7_GPIO_54	J5218	63	P3	DI	spi_miso/uart_rx	
BLSP7_GPIO_55	J5218	61	P3	DODI/ODOI	spi_cs/uart_cts/i2c_sda	
BLSP7_GPIO_56	J5218	59	P3	DO/ODOI	spi_clk/uart_rfr/i2c_scl	
BLSP8 Interface						

MSM_UART_TX	J5218	57	P3	DO	spi_mosi/uart_tx	gpio4;default uart log
MSM_UART_RX	J5218	55	P3	DI	spi_miso/uart_rx	gpio5;default uart log
BLSP8_GPIO_6	J5218	53	P3	DODI/ODOI	spi_cs/uart_cts/i2c_sda	
BLSP8_GPIO_7	J5218	51	P3	DO/ODOI	spi_clk/uart_rfr/i2c_scl	
BLSP9 Interface						
BLSP9_GPIO_49	J5218	73	P3	DO	spi_mosi/uart_tx	
BLSP9_GPIO_50	J5218	71	P3	DI	spi_miso/uart_rx	
BLSP9_GPIO_51	J5218	69	P3	DODI/ODOI	spi_cs/uart_cts/i2c_sda	
BLSP9_GPIO_52	J5218	67	P3	DO/ODOI	spi_clk/uart_rfr/i2c_scl	
BLSP10 Interface						
BLSP10_GPIO_8	J5218	81	P3	DO	spi_mosi/uart_tx	
BLSP10_GPIO_9	J5218	79	P3	DI	spi_miso/uart_rx	
BLSP10_GPIO_10	J5218	77	P3	DODI/ODOI	spi_cs/uart_cts/i2c_sda	
BLSP10_GPIO_11	J5218	75	P3	DO/ODOI	spi_clk/uart_rfr/i2c_scl	
BLSP11 Interface						
BLSP11_GPIO_58	J5218	76	P3	DO	spi_mosi/uart_tx	
BLSP11_GPIO_59	J5218	74	P3	DI	spi_miso/uart_rx	
BLSP11_GPIO_60	J5218	72	P3	DODI/ODOI	spi_cs/uart_cts/i2c_sda	
BLSP11_GPIO_61	J5218	70	P3	DO/ODOI	spi_clk/uart_rfr/i2c_scl	
BLSP12 Interface						
BLSP12_GPIO_85	J5218	64	P3	DO	spi_mosi/uart_tx	
BLSP12_GPIO_86	J5218	62	P3	DI	spi_miso/uart_rx	
BLSP12_GPIO_87	J5218	60	P3	DODI/ODOI	spi_cs/uart_cts/i2c_sda	
BLSP12_GPIO_88	J5218	58	P3	DO/ODOI	spi_clk/uart_rfr/i2c_scl	

Table 3.2-5BLSP interface definition

3.2.12 Power on Interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the device's available power sources, enable the correct source. It is longer than 1s with pressing power-on key, for power on event. And it is suggested for 3s

powering on system. Power on/off key signal can be connected to ground through J5218.83; the other power on method is: when using CBL_PWR_N pin connect to ground, insert battery or power supply, SOM will power on automatically.

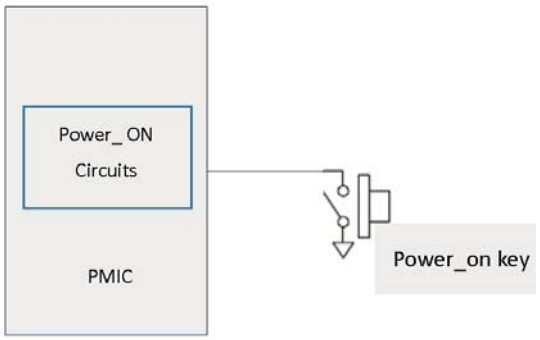

Figure 3.2-2 Power on signal

Power on Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
KYPD_PWR_N1	J5218	83	pulled up internally through a 200K resistor to 1.8V	DI	Power on/off key signal,	Low level active
CBL_PWR_N	J5218	44	pulled up internally through a 200K resistor to 1.8V	DI	Signal use for auto power on when you plug in a battery, active low, internal pull up	

Table 3.2-12Power on interface definition

3.2.13 Reset Interface

Extended press of volume key will initiate a shutdown or reset (software selectable)

- Stage 1 reset – software-configurable bark

PMIC generates interrupt, giving the soc device the opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark: Over temperature indicates system is getting too hot. PMIC watchdog indicates that it has not kicked.

- Stage 2 –software-configurable bite

If reset is ignored, PMIC will force a reset event (selectable by software).

- Stage 3 –hardware mandatory bite

The user can generate a mandatory reset by a long key press of PM_RESIN_N, or KYPD_PWR_N1, or

PM_RESIN_N + KYPD_PWR_N1.

The standalone or combination of reset triggers can also be selected as SBL by directly writing to the appropriate registers

Reset Pin						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PM_RESIN_N	J5218	85	pulled up internally to 1.8V	DI	Volume down/Reset key signal, Low active	

Table 3.2-6Reset interface definition

3.2.14 Keys Interface

KEY_GPIO can be configure to key functions as your request.

KEYs PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
KEY_VOL_UP_N	J5218	87	P3	DI	Volume up key signal, Low active	
PM_RESIN_N	J5218	85	P3	DI	Volume down key signal, Low active	
KYPD_PWR_N1	J5218	83	P3	DI	Power on/off key signal, Low active	
PM_GPIO_01	J5219	27	P3	DI	Back key signal, Low active	
PM_GPIO_02	J5219	28	P3	DI	Home key signal, Low active	

Table 3.2-7Keys interface definition

3.2.15 Sensor Interrupt Interface

All these interfaces dedicate to below sensors.

Sensor Interrupt PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
GPIO_117	J5219	29	P3	DI	Accelerometer sensor interrupt signal	

GPIO_118	J5219	30	P3	DI	GYRO Sensor interrupt	
GPIO_119	J5219	31	P3	DI	Magnetometer sensor interrupt signal	
GPIO_120	J5219	32	P3	DI	Ambient light sensor interrupt signal	
GPIO_121	J5219	33	P3	DI		
GPIO_122	J5219	34	P3	DI		
GPIO_123	J5219	35	P3	DI		
GPIO_124	J5219	36	P3	DI	Hall sensor interrupt	
GPIO_125	J5219	37	P3	DI		

Table 3.2-8Sensor interrupt definition

3.2.16 Debug UART Interface

This is interface dedicate for uart debug.

Debug UART PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
MSM_UART_TX	J5218	57	P3	DO	BLSP8 UART signals, can use for debug	
MSM_UART_RX	J5218	55	P3	DI		

Table 3.2-9Debug UART interface definition

3.2.17 Battery Interface

There is a NTC pin which is for internal battery package NTC resistor connection.

The SOM can't be monitoring battery status and charging.

Battery PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
BAT_THERM	J5218	17	2.7V	AI	Battery temperature sense input signal	10K NTC resistor to gnd; if without NTC, a 10K resistor is necessary for replaced.

Table 3.2-17 NTC interface

3.2.18 JTAG debug

The SOM supports one jtag interface for advanced debugging.

JTAG interfaces						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
JTAG_TMS	J101	1	P3			
JTAG_TCK	J101	2	P3			
JTAG_TDO	J101	3	P3			
JTAG_TDI	J101	4	P3			
JTAG_TRST_N	J101	5	P3			
KYPD_PWR_N1	J101	6	P3			
PM_RESIN_N	J101	7	P3			
GND	J101	8	P3			
JTAG_RESOUT_N	J101	9	P3			
MSM_UART_TX	J101	10	P3			
MSM_UART_RX	J101	11	P3			
VREG_S4A_1P8	J101	12	P3			
MSM_PS_HOLD	J101	13	P3			
GPIO57_FORCE_USB_BOOT	J101	14	P3			
WDOG_DISABLE	J101	15	P3			
MSM_RESOUT_N	J101	16	P3			

Table 3.2-18JTAG

3.2.19 MPPs Interface

The MPPs can be programmed to digital input/digital output/analog input/analog output/bidirectional IO/programmable current sink.

The pmi8994 device does not support the bidirectional I/O configuration; and only even-numbered MPPs can be current sinks while only odd-numbered MPPs can be analog outputs.

The PM8996 device only odd MPPs(MPP5) can be configured as analog output; only even MPPs(MPP2,MPP4,MPP6) have current sink capability.

The ADC input cannot reliably go below 0.05V or above (P3 – 0.05 V); do not exceed this range.

MPPs PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**

PMI_MPP1	J5219	7				Cannot be used as current sink
PMI_MPP2	J5219	8				Cannot be used as analog output
PM_MPP2	J5219	9				
PM_MPP5	J5219	10				Can be used as analog output
PM_MPP6	J5219	11				
PM_MPP4	J5218	42				

Table 3.2-19MPPs interface definition

3.2.20 PWMs

The SOM support PWM output, all PWM output by Light Pulse Generators.

Independently programmable duty cycle and period via LPGs (6-or 9-bit resolution) for digital dimming.

PWMs PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PM_GPIO_04	J5219	17	P3		LDP_DRV1	PM LPG
PM_GPIO_05	J5219	18	P3		LDP_DRV2	
PM_GPIO_07	J5219	20	P3		LDP_DRV3	
PM_GPIO_10	J5219	21	P3		LDP_DRV6	
PMI_MPP1	J5219	7	P3			PMI LPG
PMI_MPP2	J5219	8	P3			

Table 3.2-10PWMs and LED Current Driver interface definition

3.2.21 Antenna Interface

The SOM provides the fully-integrated WLAN, Bluetooth and GPS function.
The WLAN, Bluetooth and GPS share the antenna port with 50ohm impedance.

- WLAN supports2 × 2 multiple input, multiple output (MIMO) with two spatial streams IEEE802.11 a/b/g/n/ac WLAN standards.
- Supports Bluetooth 4.2 + HS enabling seamless integration of WLAN/Bluetooth and low energy technology.
- Supports GPS, GLONASS, and COMPASS operation.

Antenna interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
Antenna 1	J5201			IO	Antenna 1 supports WIFI 2.4G/5G &BT	Chain0
Antenna 2	J5202			IO	Antenna 2 supports WIFI 2.4G/5G	Chain1
Antenna 3	J5222			IO	Antenna GPS	

Table 3.2-21Antenna interface definition

3.2.22 GPIO

The SOM supports the GPIOs which are multi function with others, such as blsp, i2s and others. It can be configured by different software setting. Some GPIOs can be used as APQ power management interrupt which can wake the system up.

GPIO							
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Interrupt**	**Description**	**Notes**
GPIO_73	J5218	19	P3	DI/DO	YES		
GPIO_21	J5218	21	P3	DI/DO			
GPIO_12	J5218	23	P3	DI/DO			
GPIO_38	J5218	25	P3	DI/DO	YES		
GPIO_72	J5218	35	P3	DI/DO			
GPIO_71	J5218	37	P3	DI/DO	YES		
GPIO_70	J5218	39	P3	DI/DO			
GPIO_69	J5218	41	P3	DI/DO			
GPIO_64	J5218	49	P3	DI/DO	YES		
BLSP8_GPIO_7	J5218	51	P3	DI/DO			
BLSP8_GPIO_6	J5218	53	P3	DI/DO			
BLSP7_GPIO_56	J5218	59	P3	DI/DO	YES		
BLSP7_GPIO_55	J5218	61	P3	DI/DO			
BLSP7_GPIO_54	J5218	63	P3	DI/DO	YES		
BLSP7_GPIO_53	J5218	65	P3	DI/DO	YES		
BLSP9_GPIO_52	J5218	67	P3	DI/DO			
BLSP9_GPIO_51	J5218	69	P3	DI/DO			
BLSP9_GPIO_50	J5218	71	P3	DI/DO	YES		

BLSP9_GPIO_49	J5218	73	P3	DI/DO			
BLSP10_GPIO_11	J5218	75	P3	DI/DO	YES		
BLSP10_GPIO_10	J5218	77	P3	DI/DO			
BLSP10_GPIO_9	J5218	79	P3	DI/DO	YES		
BLSP10_GPIO_8	J5218	81	P3	DI/DO			
GPIO_24	J5218	89	P3	DI/DO	YES		
GPIO_23	J5218	91	P3	DI/DO			
BLSP6_GPIO_28	J5218	93	P3	DI/DO			
BLSP6_GPIO_27	J5218	95	P3	DI/DO			
BLSP6_GPIO_26	J5218	97	P3	DI/DO	YES		
BLSP6_GPIO_25	J5218	99	P3	DI/DO			
GPIO_34	J5218	48	P3	DI/DO	YES		
GPIO_33	J5218	50	P3	DI/DO			
GPIO_32	J5218	52	P3	DI/DO			
GPIO_31	J5218	54	P3	DI/DO			
GPIO_30	J5218	56	P3	DI/DO			
BLSP12_GPIO_88	J5218	58	P3	DI/DO			
BLSP12_GPIO_87	J5218	60	P3	DI/DO			
BLSP12_GPIO_86	J5218	62	P3	DI/DO	YES		
BLSP12_GPIO_85	J5218	64	P3	DI/DO			
GPIO_63	J5218	66	P3	DI/DO	YES		
GPIO_62	J5218	68	P3	DI/DO	YES		
BLSP11_GPIO_61	J5218	70	P3	DI/DO	YES		
BLSP11_GPIO_60	J5218	72	P3	DI/DO	YES		
BLSP11_GPIO_59	J5218	74	P3	DI/DO	YES		
BLSP11_GPIO_58	J5218	76	P3	DI/DO	YES		
BLSP5_GPIO_84	J5218	80	P3	DI/DO			
BLSP5_GPIO_83	J5218	82	P3	DI/DO			
BLSP5_GPIO_82	J5218	84	P3	DI/DO	YES		
BLSP5_GPIO_81	J5218	86	P3	DI/DO			
GPIO_80	J5218	88	P3	DI/DO	YES		
GPIO_79	J5218	90	P3	DI/DO	YES		
GPIO_78	J5218	92	P3	DI/DO	YES		
GPIO_77	J5218	94	P3	DI/DO	YES		
GPIO_76	J5218	96	P3	DI/DO			

GPIO_75	J5218	98	P3	DI/DO			
GPIO_74	J5218	100	P3	DI/DO			
GPIO_130	J5221	76	P3	DI/DO			
GPIO_131	J5221	78	P3	DI/DO	YES		
GPIO_132	J5221	80	P3	DI/DO	YES		
GPIO_114	J5221	82	P3	DI/DO			
GPIO_115	J5221	84	P3	DI/DO	YES		
GPIO_116	J5221	86	P3	DI/DO	YES		
GPIO_29	J5221	23	P3	DI/DO			
GPIO_22	J5221	99	P3	DI/DO	YES		
PMI_GPIO2	J5219	1	1.8V	DI/DO			
PMI_GPIO5	J5219	2	1.8V	DI/DO			
PMI_GPIO6	J5219	3	1.8V	DI/DO			From PMI8994
PMI_GPIO9	J5219	4	1.8V	DI/DO			
PMI_GPIO10	J5219	5	1.8V	DI/DO			
PM_GPIO_04	J5219	17	1.8V	DI/DO			
PM_GPIO_05	J5219	18	1.8V	DI/DO			
PM_GPIO_06	J5219	19	1.8V	DI/DO			From PM8996
PM_GPIO_07	J5219	20	1.8V	DI/DO			
PM_GPIO_10	J5219	21	1.8V	DI/DO			
BLSP1_GPIO_0	J5219	22	P3	DI/DO			
BLSP1_GPIO_1	J5219	23	P3	DI/DO	YES		
BLSP1_GPIO_2	J5219	24	P3	DI/DO			
BLSP1_GPIO_3	J5219	25	P3	DI/DO			
GPIO_107	J5219	26	P3	DI/DO			
PM_GPIO_01	J5219	27	1.8V	DI/DO			From PM8996
PM_GPIO_02	J5219	28	1.8V	DI/DO			
GPIO_117	J5219	29	P3	DI/DO	YES		
GPIO_118	J5219	30	P3	DI/DO	YES		
GPIO_119	J5219	31	P3	DI/DO	YES		
GPIO_120	J5219	32	P3	DI/DO	YES		
GPIO_121	J5219	33	P3	DI/DO	YES		
GPIO_122	J5219	34	P3	DI/DO	YES		
GPIO_123	J5219	35	P3	DI/DO	YES		
GPIO_124	J5219	36	P3	DI/DO	YES		

GPIO_125	J5219	37	P3	DI/DO	YES		
PM_GPIO_14	J5220	19	1.8V	DI/DO			From PM8996
PM_GPIO_22	J5220	20	1.8V	DI/DO			
GPIO_126	J5220	21	P3	DI/DO	YES		
PMI_GPIO3	J5220	22	P3	DI/DO			
BLSP3_GPIO_48	J5220	23	P3	DI/DO			
BLSP3_GPIO_47	J5220	24	P3	DI/DO			
GPIO_96	J5220	26	P3	DI/DO			
GPIO_95	J5220	27	P3	DI/DO	YES		
GPIO_94	J5220	28	P3	DI/DO			
GPIO_93	J5220	29	P3	DI/DO			
GPIO_92	J5220	30	P3	DI/DO	YES		
GPIO_91	J5220	31	P3	DI/DO	YES		
GPIO_90	J5220	32	P3	DI/DO			
GPIO_40	J5220	33	P3	DI/DO	YES		
GPIO_39	J5220	34	P3	DI/DO			
GPIO_89	J5220	35	P3	DI/DO			

Table 3.2-22GPIOs

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

The SOM needs to be desinged in the operatin conditons which is shown as below table.

Parameter	Min	Typical	Max	Units
Input Power voltage				
VBAT	3.8	4.0	4.2	V
ESD				
ESD-HBM model rating	±2k			KV
ESD-CDM model rating	±4k			KV

Table 4.1-1Absolute rating condition

***Notes**: for the ESD, it will be valid and available only when the module is fully tested and approved in the Initial*

Production stage.

4.2 Operating Conditions

The SOM needs to be desinged in the operatin conditons which is shown as below table.

Parameters	Min	Typical	Max	Units
Input Power voltage				
VBAT	+3.8	4.0	+4.2	V
VBAT	0.1	1.0	3	A
Thermal conditions				
Operating temperature	-10	25	55	℃
Storage temperature	-10	25	55	℃

Table 4.2-1Operating condition

Note: *For the thermal conditons, operatin and storage min and max temperature is only when the module is fully tested and approved in the Initial Production stage.*

4.3 Output Power

The SOM provide power supply for external device, such as SD card, IO voltage,Below map show the details.

Function	Default voltage(V)	Programble range(V)	Rated current(mA)	Default ON	Expected use
VREG_S4A_1P8	+1.8	NA	300	Y	power output for external io voltage and 1.8V IO pull up voltage;
VREG_L21A_2P95	+2.95	+1.62--+3.6	300	Y	Power output for SD card

Table 4.3-1Output power

4.4 Digital-logic characteristics

The digital I/O's performance depeds on its pad type, usage, and power supply voltage.The SOM IO voltage level is the same with P3 except the SD card and analog input/output. The I2C, USB,MIPI and UART comply with the satndards.

4.4.1 Digital GPIO characteristics

The followint table shows the digital GPIO characteristics:

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt,	0.7* P3	P3+0.3	V
VIL	Low-level input voltage, CMOS/Schmitt,	-0.3	0.3* P3	V
VSHYS	Schmitt hysteresis voltage	300	-	mV
VOH	High-level output voltage, CMOS	VREG_S4A_1P8-0.45	VREG_S4A_1P8	V
VOL	Low-level output voltage, CMOS	0.0	0.45	V
RPULL-UP	Pull-up resistance	20 K	60 K	Ω
RPULL-DOWN	Pull-down resistance	60 K	20 K	Ω

Table 4.4-1 Digital IO voltage performance

4.4.2 SD card digital I/O characteristics

The SD card is powered by P2 supply; the power is 1.8V and 2.95V.the following table shows the SD card digital I/O characteristics:

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	1.27/2.065	-	2.1/3.25	V
VIL	Low-level input voltage	-0.3/-0.3	-	0.45/0.74	V
VHYS	Schmitt hysteresis voltage	100	-	-	mV
RPULL-UP	Pull-up resistance	10 K	-	100K	Ω
RPULL-DOWN	Pull-down resistance	10 K	-	100K	Ω
RKEEPER-UP	Keeper-up resistance	10 K	-	100K	Ω
RKEEPER-DOWN	Keeper-down resistance	10 K	-	100K	Ω
VOH	High-level output voltage	1.4/2.21	-	1.8/2.95	V

VOL	Low-level output voltage	0/0	-	0.225/1.091	V

Table 4.4-2SD digital IO voltage performance (1.8V/2.95V)

4.5 MIPI

The SOM supports the MIPI interface and comply with MIPI standards.

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for DPHY v1.2	None

Table 4.5-1 MIPI_DSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v1.3	RAW7 not supported DPCM predictor 2 not supported
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	None

Table 4.5-1 MIPI_CSI

4.6 USB

The SOM supports USB standards and exceptions.

Applicable standard	Feature exceptions	APQ variation
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2	Operating voltages, system clock, and VBUS
UTMI + Low Pin Interface (ULPI) Specification (October 20, 2004 Revision 1.1 or later)	None	None
On-The-Go and Embedded Host Supplement to theUSB 3.0 Specification (May 10, 2012, Revision 1.1 orlater)	None	None

Table 4.6-1USB

4.7 PCIe

The SOM supports PCIe standards and exceptions

Applicable standard	Feature exceptions	APQ variation
PCI Express Specification, Revision 2.1 (March 4, 2009 or later)	None	None

Table 4.7-1PCIe

4.8 HDMI

The SOM supports HDMI standards and exceptions

Applicable standard	Feature exceptions	APQ variation
HDMI Specification Version 2.0	None	None

Table 4.8-1HDMI

4.9 SLIMbus

The SOM supports SLIMbus HDMI standards and exceptions

Applicable standard	Feature exceptions	APQ variation
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None	None

Table 4.9-1SLIMbus

4.10 SDIO

The SOM Supports SD standards and exceptions

Applicable standard	Feature exceptions
Embedded Multimedia Card (eMMC) Specification version 5.1	None
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

Table 4.10-1 SDIO

4.11 I2S

The SOMI2S standards and exceptions:

Legacy I2S interfaces for primary and secondary microphones and speakers.
The multiple I2S (MI2S) interface for microphone and speaker functions, including 7.1 audio for HDMI.
It is supports both master and slave mode.
Supports 16, 24, or 32-bit resolution audio samples
Supports 8,16,32,48,96 and192 kHz sampling rate in Master mode, and all standard sample rates in Slave mode. Supports16-bit and 24-bit data formats in standard I2S mode, and 24-bit left-justified (24-bit data in 32-bit frame left-justified, LSBs are padded with 0s).
Maximum clock frequency supported 12.288 MHz.
An additional pin can be used for a master clock, supplied by the MSM device, the master clock is often used in the external devices to drive their oversampling logic. The LPASS clock controller can provide master clocks from independent clock dividers to the I2S bit-clock dividers.

Applicable standard	Feature exceptions	MSM variations
Philips I2S Bus Specifications revised June 5, 1996	None	When an external SCK clock is used, a duty cycle between45% to 55% is required.

Table 4.11-1 I2S

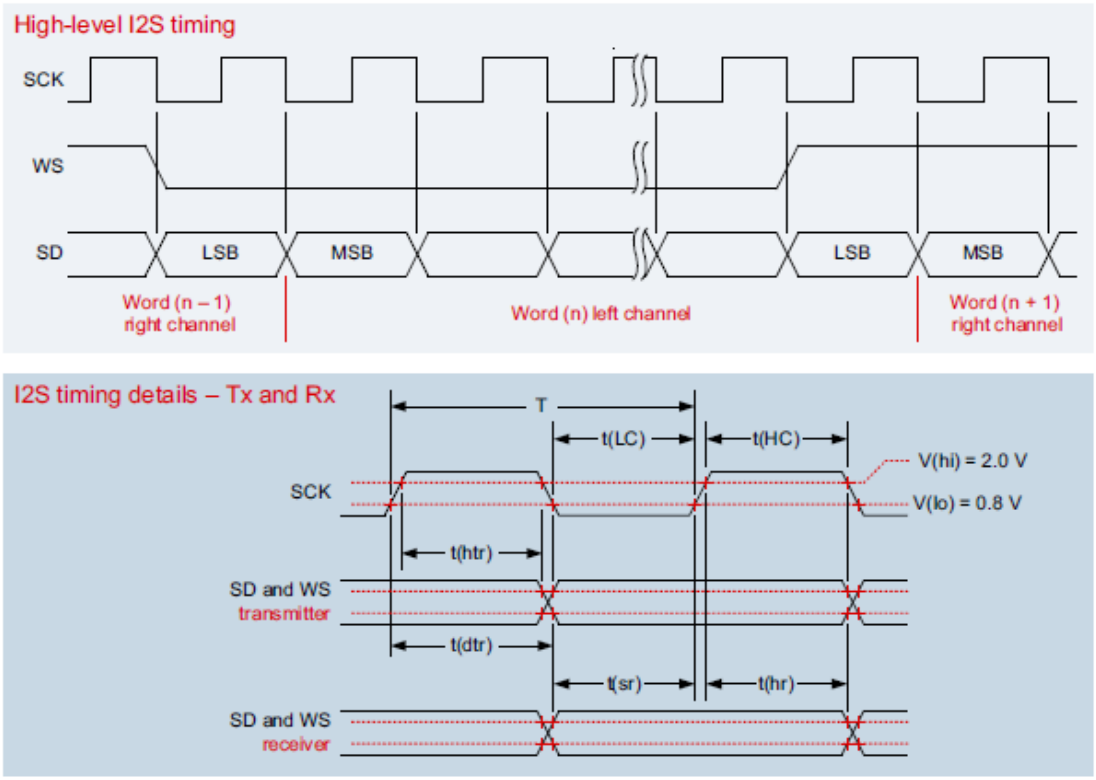

Figure 4.11-1I2S timing diagram

The word-select signal is a 50% duty cycle signal. Data is delayed 1 bit-clock, relative to the word select. Data outputs are launched on the falling edge of the clock, and inputs data are captured on the rising edge of the clock by the receiver.
I2S samples are 2's complement values, and the MSB is transmitted first allowing the transmitter and receiver to support different number of bits per sample.
The left channel is transmitted when the word select is low, and the right channel is transmitted when the word select is high

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
Frequency		–	–	–	12.288	MHz
T	Clock period	–	81.380	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	16.276	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	65.100	ns
t(htr)	SD and WS output hold time	–	0	–	–	ns
Using external SCK						
Frequency		–	–	–	12.288	MHz
T	Clock period	–	81.380	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	16.276	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	65.100	ns
t(htr)	SD and WS output hold time	–	0	–	–	ns

Table 4.11-2 I2S Timing

4.12 I2C

The SOMI2C standards and exceptions:

Applicable standard	Feature exceptions
I2C Specification, version 3.0	None

Table 4.12-1 I2C

4.13 SPI

The SOM supports **SPI** standards and exceptions: IT IS supports SPI as a master only.

4.14 Mpps

MPPs can be configured any of the functions specified within Table 4.14-1

Function	Min	Typ	Max	Units	Expected use
MPP configured as digital input					
Logic high-input	0.65 · VM[1]	-	-	V	
Logic low-input	-	-	0.35 ·VM[1]	V	
MPP configured as digital output					
Logic high-output	VM[1] – 0.45	-	VM[1]	V	
Logic low-output	0	-	0.45	V	
Drive strength Logic high (V_M > 2.5 V) Logic high (V_M < 2.5 V) Logic low	 5.1 3.3 5.9	 7.3 4.9 11.3	 15.2 9.9 36.0	mA	
MPP configured as analog input					
Input current	-	-	100	mA	
MPPs configured as current sinks					
Output current	0	-	40	mA	

Table 4.14-1Mpps

Notes:

VM1 = 1.8V

4.15 Power Consumption

Power Consumption					
S/N	**Test Items and Test Condition**		UNIT	**DUT**	
				average value	**data range**
1	**Normal Operation Current (Play Movie)** -Wi-Fi off, BT off - Vol Max, no LCD, no Camera	4K	mA	382	245--634
		1080P		305	270--545
2	**Normal Operation Current (Idle mode)** **-** Restart the device - At Home Page - No LCD. No Camera	WIFI ON	mA	104	64.7--416
		WIFi OFF	mA	71	63.1--99
3	**Normal Operation Current (Sleep Mode)** - No LCD. No camera	WIFI ON	mA	24	12.4--239
		WIFi OFF	mA	6	5.3--6.1
4	**Normal Operation Current** (online Play Movie 1080P Movie) - No LCD. No camera	WIFI On	mA	485	222---989
5	**Run in CPU Max Loading(1.5G+2.1G)**	WIFI On	mA	2389	1506--3287
6	**Camera Record** no LCD	WIFI Off	mA	NA	NA
7	**Leakage current**	-	uA	178	<200uA

Table 4.15-1Power Consumption (Without LCD/Camera)

4.16 Thermal(TBD)

4.17 RF Performance

4.17.1 GPS Performance

GPS RF Performance	
Conditions : VBAT=4.0V ; signal source=-130dBm/Hz,Temp:25°C	
C/N0	40dB

Table 4.17-4 GPS Performance

5 PIN Summary

5.1 J5218 BTB Connector

Pin	Signal Name		Pin	Signal Name
1	VBATT		2	VBUS_USB_IN
3	VBATT		4	VBUS_USB_IN
5	VBATT		6	USB3_HS_USB_ID
7	VBATT		8	VREG_S4A_1P8
9	VBATT		10	GND
11	VBATT		12	MIPI_DSI0_CLK_P_CON
13	VREG_L21A_2P95		14	MIPI_DSI0_CLK_N_CON
15	VREG_L21A_2P95		16	GND
17	BAT_THERM		18	MIPI_DSI0_LAN3_P_CON
19	GPIO_73		20	MIPI_DSI0_LAN3_N_CON
21	GPIO_21		22	GND
23	GPIO_12		24	MIPI_DSI0_LAN2_P_CON
25	GPIO_38		26	MIPI_DSI0_LAN2_N_CON
27	GND		28	GND
29	GND		30	MIPI_DSI0_LAN0_P_CON
31	GND		32	MIPI_DSI0_LAN0_N_CON
33	GND		34	GND
35	GPIO_72		36	MIPI_DSI0_LAN1_P_CON
37	GPIO_71		38	MIPI_DSI0_LAN1_N_CON
39	GPIO_70		40	GND
41	GPIO_69		42	PM_MPP4
43	GND		44	CBL_PWR_N
45	PM_GPIO_15		46	VCOIN

47	GND		48	GPIO_34
49	GPIO_64		50	GPIO_33
51	BLSP8_GPIO_7		52	GPIO_32
53	BLSP8_GPIO_6		54	GPIO_31
55	MSM_UART_RX		56	GPIO_30
57	MSM_UART_TX		58	BLSP12_GPIO_88
59	BLSP7_GPIO_56		60	BLSP12_GPIO_87
61	BLSP7_GPIO_55		62	BLSP12_GPIO_86
63	BLSP7_GPIO_54		64	BLSP12_GPIO_85
65	BLSP7_GPIO_53		66	GPIO_63
67	BLSP9_GPIO_52		68	GPIO_62
69	BLSP9_GPIO_51		70	BLSP11_GPIO_61
71	BLSP9_GPIO_50		72	BLSP11_GPIO_60
73	BLSP9_GPIO_49		74	BLSP11_GPIO_59
75	BLSP10_GPIO_11		76	BLSP11_GPIO_58
77	BLSP10_GPIO_10		78	GPIO57_FORCE_USB_BOOT
79	BLSP10_GPIO_9		80	BLSP5_GPIO_84
81	BLSP10_GPIO_8		82	BLSP5_GPIO_83
83	KYPD_PWR_N1		84	BLSP5_GPIO_82
85	PM_RESIN_N		86	BLSP5_GPIO_81
87	PM_GPIO_03		88	GPIO_80
89	GPIO_24		90	GPIO_79
91	GPIO_23		92	GPIO_78
93	BLSP6_GPIO_28		94	GPIO_77
95	BLSP6_GPIO_27		96	GPIO_76
97	BLSP6_GPIO_26		98	GPIO_75
99	BLSP6_GPIO_25		100	GPIO_74

5.2 J5221 BTB Connector

Pin	Signal Name		Pin	Signal Name
1	GND		2	GND
3	CAM_MCLK0		4	MSM_HDMI_TX0_P
5	GND		6	MSM_HDMI_TX0_M
7	CAM_MCLK1		8	GND
9	GND		10	MSM_HDMI_TCLK_P
11	CAM_MCLK2		12	MSM_HDMI_TCLK_M
13	GND		14	GND
15	CCI_I2C_SDA0		16	MSM_HDMI_TX2_P
17	CCI_I2C_SCL0		18	MSM_HDMI_TX2_M
19	CCI_I2C_SDA1		20	GND
21	CCI_I2C_SCL1		22	MSM_HDMI_TX1_P
23	GPIO_29		24	MSM_HDMI_TX1_M
25	GND		26	GND
27	MIPI_CSI1_CLK_N		28	MIPI_CSI0_CLK_N
29	MIPI_CSI1_CLK_P		30	MIPI_CSI0_CLK_P
31	GND		32	GND
33	MIPI_CSI1_LANE0_N		34	MIPI_CSI0_LANE0_N
35	MIPI_CSI1_LANE0_P		36	MIPI_CSI0_LANE0_P
37	GND		38	GND
39	MIPI_CSI1_LANE1_N		40	MIPI_CSI0_LANE1_N
41	MIPI_CSI1_LANE1_P		42	MIPI_CSI0_LANE1_P
43	GND		44	GND
45	MIPI_CSI1_LANE2_N		46	MIPI_CSI0_LANE2_N
47	MIPI_CSI1_LANE2_P		48	MIPI_CSI0_LANE2_P
49	GND		50	GND
51	MIPI_CSI1_LANE3_N		52	MIPI_CSI0_LANE3_N
53	MIPI_CSI1_LANE3_P		54	MIPI_CSI0_LANE3_P

55	GND		56	GND
57	USB2_HS_D_P		58	USB3_SS_RX0_P
59	USB2_HS_D_M		60	USB3_SS_RX0_M
61	GND		62	GND
63	PCIE1_REFCLK_N		64	USB3_SS_TX0_P
65	PCIE1_REFCLK_P		66	USB3_SS_TX0_M
67	GND		68	GND
69	PCIE1_MSM_RX_N		70	USB3_HS_D_P
71	PCIE1_MSM_RX_P		72	USB3_HS_D_M
73	GND		74	GND
75	PCIE1_MSM_TX_N		76	GPIO_130
77	PCIE1_MSM_TX_P		78	GPIO_131
79	GND		80	GPIO_132
81	PCIE2_REFCLK_N		82	GPIO_114
83	PCIE2_REFCLK_P		84	GPIO_115
85	GND		86	GPIO_116
87	PCIE2_MSM_RX_N		88	GND
89	PCIE2_MSM_RX_P		90	SDC2_SDCARD_D3
91	GND		92	SDC2_SDCARD_CMD
93	PCIE2_MSM_TX_N		94	SDC2_SDCARD_CLK
95	PCIE2_MSM_TX_P		96	SDC2_SDCARD_D0
97	GND		98	SDC2_SDCARD_D1
99	GPIO_22		100	SDC2_SDCARD_D2

5.3 J5219 ZIF Connector

Pin	Signal Name		Pin	Signal Name
1	PMI_GPIO2		26	GPIO_107

2	PMI_GPIO5		27	PM_GPIO_01
3	PMI_GPIO6		28	PM_GPIO_02
4	PMI_GPIO9		29	GPIO_117
5	PMI_GPIO10		30	GPIO_118
6	GND		31	GPIO_119
7	PMI_MPP1		32	GPIO_120
8	PMI_MPP2		33	GPIO_121
9	PM_MPP2		34	GPIO_122
10	PM_MPP5		35	GPIO_123
11	PM_MPP6		36	GPIO_124
12	GND		37	GPIO_125
13	PM_GPIO_17		38	SPI_CS_N_MAG
14	GND		39	SSC_PWR_EN
15	BBCLK2		40	SSC_I2C_3_SDA
16	GND		41	SSC_I2C_3_SCL
17	PM_GPIO_04		42	SSC_I2C_2_SDA
18	PM_GPIO_05		43	SSC_I2C_2_SCL
19	PM_GPIO_06		44	SSC_SPI_1_CS_N
20	PM_GPIO_07		45	SSC_SPI_1_CLK
21	PM_GPIO_10		46	SSC_SPI_1_MOSI
22	BLSP1_GPIO_0		47	SSC_SPI_1_MISO
23	BLSP1_GPIO_1		48	SSC_SPI_3_CLK
24	BLSP1_GPIO_2		49	SSC_SPI_3_CS_N
25	BLSP1_GPIO_3		50	SSC_SPI_3_MOSI
			51	SSC_SPI_3_MISO

5.4 J5220 ZIF Connector

Pin	Signal Name		Pin	Signal Name
1	GND		26	GPIO_96
2	MIPI_CSI2_LAN3_P		27	GPIO_95
3	MIPI_CSI2_LAN3_N		28	GPIO_94
4	GND		29	GPIO_93
5	MIPI_CSI2_LAN2_P		30	GPIO_92
6	MIPI_CSI2_LAN2_N		31	GPIO_91
7	GND		32	GPIO_90
8	MIPI_CSI2_LAN0_P		33	GPIO_40
9	MIPI_CSI2_LAN0_N		34	GPIO_39
10	GND		35	GPIO_89
11	MIPI_CSI2_LAN1_P		36	GND
12	MIPI_CSI2_LAN1_N		37	MIPI_DSI1_LANE3_N_CON
13	GND		38	MIPI_DSI1_LANE3_P_CON
14	MIPI_CSI2_CLK_P		39	GND
15	MIPI_CSI2_CLK_N		40	MIPI_DSI1_LANE0_N_CON
16	GND		41	MIPI_DSI1_LANE0_P_CON
17	CAM_MCLK3		42	GND
18	GND		43	MIPI_DSI1_LANE2_N_CON
19	PM_GPIO_14		44	MIPI_DSI1_LANE2_P_CON
20	PM_GPIO_22		45	GND
21	GPIO_126		46	MIPI_DSI1_CLK_N_CON
22	PMI_GPIO3		47	MIPI_DSI1_CLK_P_CON
23	BLSP3_GPIO_48		48	GND
24	BLSP3_GPIO_47		49	MIPI_DSI1_LANE1_N_CON
25	GND		50	MIPI_DSI1_LANE1_P_CON
			51	GND

5.5 J101 JTAG Connector

Pin	Signal Name		Pin	Signal Name
1	JTAG_TMS		9	JTAG_RESOUT_N
2	JTAG_TCK		10	MSM_UART_TX
3	JTAG_TDO		11	MSM_UART_RX
4	JTAG_TDI		12	VREG_S4A_1P8
5	JTAG_TRST_N		13	MSM_PS_HOLD
6	KYPD_PWR_N1		14	GPIO_57_FORCE_USB_BOOT
7	PM_RESIN_N		15	WDOG_DISABLE
8	GND		16	MSM_RESOUT_N

FCC Caution:

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment .This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

—Reorient or relocate the receiving antenna.

—Increase the separation between the equipment and receiver.

—Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

—Consult the dealer or an experienced radio/TV technician for help.

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: **—**Contains FCC ID: **2AOHHTURBOXSOMD820.**

ISEDC Warning:

This device complies with Innovation, Science, and Economic Development Canad licence-exempt RSS standard(s). Operation is subject to the following two conditions:

(1) this device may not cause interference, and
(2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d' Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :
(1) l'appareil nedoit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

This Class B digital apparatus complies with Canadian ICES-003.
Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.
The device is compliance with RF exposure guidelines, users can obtain Canadian information on RF exposure and compliance.The minimum distance from body to use the device is 20cm.
Le présent appareil est conforme
Après examen de ce matériel aux conformité ou aux limites d'intensité de champ RF,
les utilisateurs peuvent sur l'exposition aux radiofréquences et la conformité and compliance d'acquérir les informations correspondantes. La distance minimale du corps à utiliser le dispositif est de 20cm.

Per RSS GEN section 3.21 requirement, The module must be labeled with its own certification number, and, if the certification number is not visible when the module is installed inside a host device, then the host device into which the module is installed must also display a label referring to the enclosed module. For details as follows:
Contains transmitter module IC: 23465-TURBOX820
where 23465-TURBOX820 is the module's certification number