SLM927 Hardware Design Manual

Release Date: February 2023
Controlled File Name: SLM927 Hardware Design Manual
Controlled Version Number: V1.01
Publisher: Fujian LANDI Commercial Equipment Co., Ltd.

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Logo	Requirements
	When you are at a hospital or medical facility, observe the restrictions on using your phone. If necessary, please turn off the terminal or mobile phone, otherwise the medical device may malfunction due to radio frequency interference.
	Turn off the wireless terminal or mobile phone before boarding. To prevent interference with the communication system, wireless communication equipment is prohibited on the aircraft. Ignoring the above will violate local laws and may result in a flight accident.
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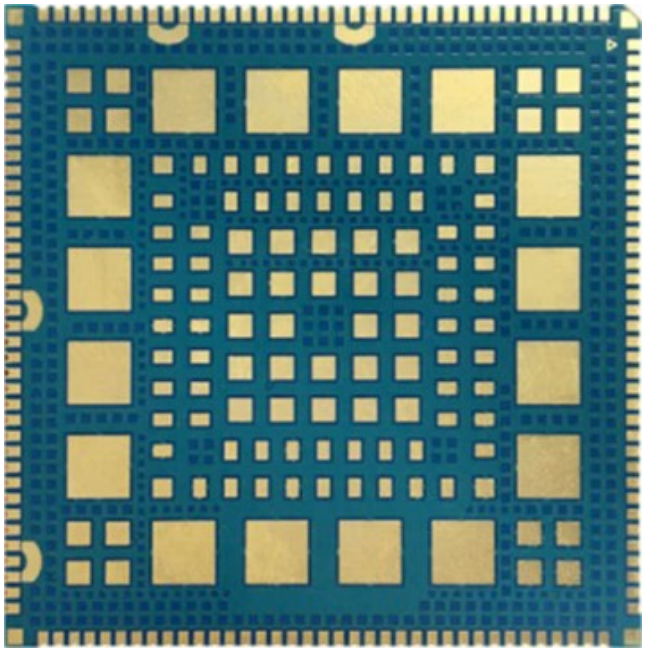
	GSM mobile terminals operate under RF signals and cellular networks, but are not guaranteed to be connected in all situations. For example, there is no credit or invalid SIM card. When in this situation and need emergency services, remember to use an emergency call. In order to be able to call and receive calls, the mobile terminal must be powered on and in a service area where the mobile signal is strong enough. Emergency calls are not allowed when certain network services or telephony features are in use, such as feature locks, keyboard locks. These functions should be removed before using an emergency call. Some networks require effective SIM card support.

SLM927 Hardware Design Manual _V1.01



Foreword

Thanks for using the SLM927 module provided by LANDI. This product can provide data communication services. Please read the design manual carefully before use, it will help you fully understand the function of the module.

The company is not responsible for property damage or personal injury caused by the user's abnormal operation. Users are requested to develop corresponding products according to the technical specifications and reference designs in the manual. Also pay attention to the general safety precautions you should be aware of when using mobile products.

Before making a statement, the company has the right to modify the contents of this manual according to the needs of technological development.

Content

Revision History

Dates	Version	Change Description	Author
2023-02	1.00	Initial establishment	Hardware Department
2023-07	1.01	Update the pin correspondence in Table 4.6	Hardware Department

1. Introduction

This document describes the hardware application interface of the module, including circuit connections and RF interfaces for relevant applications. This document can help users quickly understand the interface definition, electrical performance and structural dimensions of the module in detail. Combined with this document and other application documents, users can quickly use the module to design mobile communication applications.

2. Module Overview

SLM927 series core board, the main chip is Qualcomm Snapdragon 600 series SM6225, the CPU adopts 6nm process technology, built-in quad-core Cortex-A73 and quad-core Cortex-A53. The support memory type is UMCP or EMCP.

SLM927 module is suitable for TD-LTE/FDD-LTE/WCDMA/ multiple network standards ofbroadband intelligent wireless communication module.

SLM927 module can support the working frequency band ((take the Eurasian version as an example) :

- TDD-LTE: B41
- FDD-LTE: B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/71
- WCDMA: B2/B4/B5

The SLM927 provides voice, SMS, address book, WiFi, BT and GPS capabilities while providing high-speed broadband data access; It can be widely used in VR Camera, intelligent robot, video surveillance, security, vehicle equipment, intelligent platform handheld terminal and other products

The physical interface of the module is 276 PIN pad, which provides the following hardware interface:

- Two 1.8V UART interfaces, of which UART1 supports four wires
- One LCD interface (MIPI-DSI)
- Three Camera interface (MIPI-CSI)
- One USB2.0 interface + One USB3.1 interface
- Three analog MIC input interfaces (with integrated bias circuit)
- Three analog audio output (earphone, headphone, AUX)
- One I2S port
- Two (U)SIM card ports
- GPIO port
- Five I2C interfaces
- One SPI interfaces
- One SD card interface
- Support GNSS, WiFi, Bluetooth 4.0

Note: The number of functional interfaces is based on the default function of the interface, excluding the reuse function of the BLSP interface.

2.1. Main Features of the Module

Table 2.1: Main characteristics of the module

Product Features	Description
Platform	Qualcomm SM6225
CPU	Quad-core Cortex-A73, quad-core Cortex-A53
GPU	Adreno
System memory	64GB eMMC+4GB LPDDR4X (Default, compatible with other capacities)
Operating system	Android 13
Size	41x41x1mm, 148 PIN LCC +128 PIN LGA

Network frequency bands (Take the Eurasian version as an example)		TDD-LTE: B41 FDD-LTE: B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B66/71 WCDMA:B2/B4/B5	
Wi-Fi		WCN3988: IEEE 802.11a/b/g/n/ac 2.4G&5G	
Bluetooth		BT 4.0	
GNSS		GPS/Beidou/Glonass/Galileo	
Data Access	TD-LTE	Cat4 TD-LTE 117/30Mbps	
	FDD-LTE	Cat4 FDD-LTE 150/50Mbps	
	DC-HSPA+	42/11.2 Mbps	
SIM		DSDS Dual card Dual standby (2.95V/1.8V) Support SIM hot swappable L/W/G/T+G L/W/G/T+W L/W/G/T+1X L/EVDO/CDMA1X+G Dual CDMA cards are not supported	
Display		Up to FHD+@90Hz	
		LCD Size: User defined	
		Interface: MIPI DSI 4-lane;	
Camera		Interface: Supports three sets of Csis, each 4-Lane	
		Triple camera: 13MP+13MP+5MP at 30 fps ZSL Dual camera: 25MP+5MP, 16MP+16MP at 30 fps ZSL Single camera: 32 MP at 30 fps ZSL	
Video		Video decode	1080p60 8-bit HEVC/H.264/H.265/VP9
		Video encode	1080p60 8-bit HEVC/H.264/H.265
		Decode+ Encode	1080p30 decode+1080p30 encode
Input device		Buttons (on/off button, reset button, volume plus/minus button, HOME button)	
		Capacitive TP	
Reset		Hard reset supported	
Application interface		Interface name	Main function description
		VPH_PWR	3 PIN, module power input, 3.5V ~ 4.2V, typical value 3.8V
		SDIO *1	SD3.0
		USB/USB3.1	OTG support (OTG power supply needs external connection) FORCE_USB_BOOT (forced USB boot for emergency downloads)
		BLSP ports	7 QUP ports, multiplexed serial interface functions
		ADC*2	Support
		VCOIN	Real Time clock backup battery
		RF interface	Multimode LTE main antenna Multimode LTE diversity antenna GPS antenna 2.4G/5G WiFi/BT antenna

	Audio	Three analog MIC inputs One AUX output (external audio PA required) One handset output One stereo headphone output One I2S signal

3. Module package

3.1. Pin Distribution Diagram

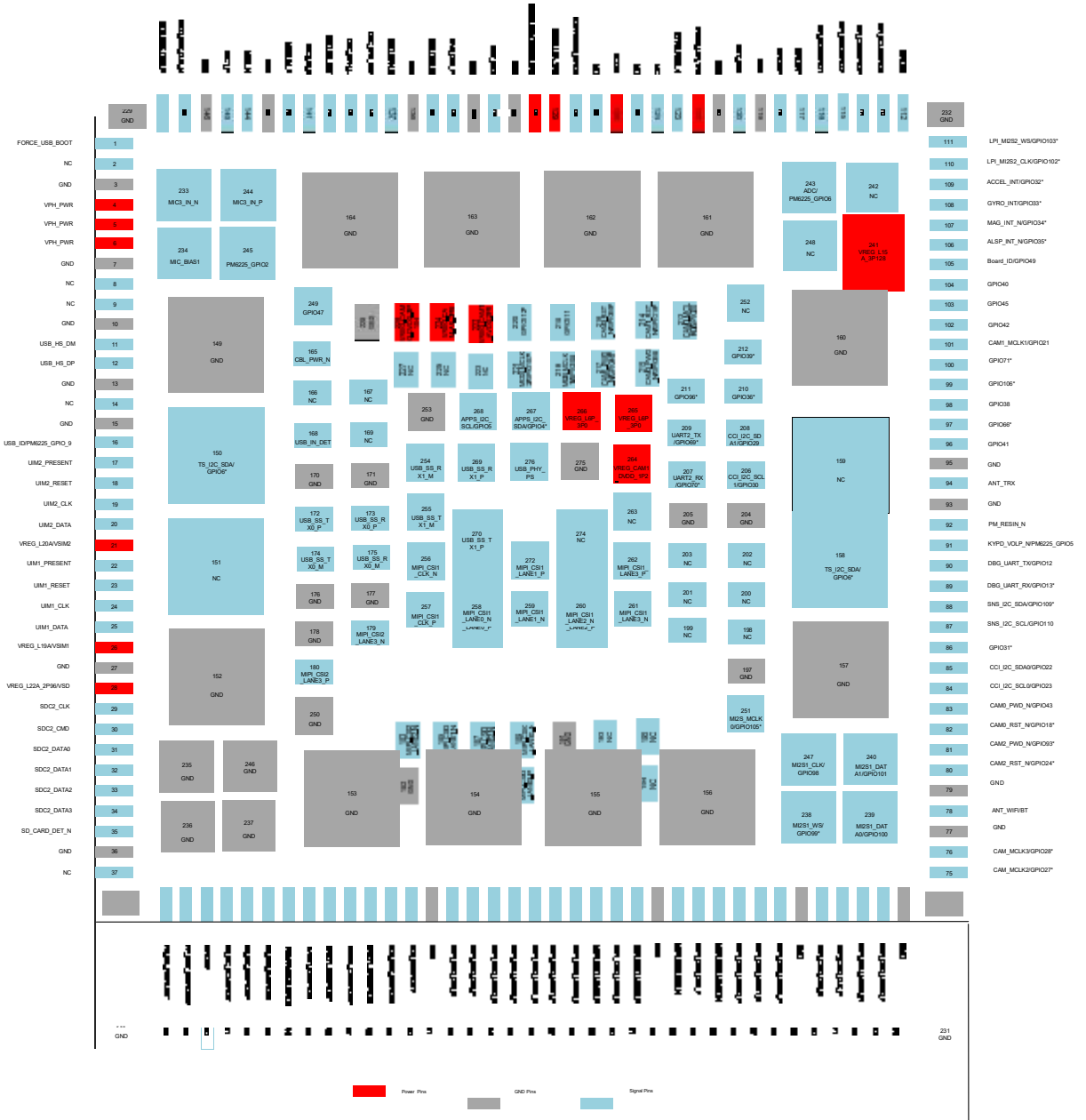


Figure 3.1 Pin diagram of module (top view)

3.2. Description of Module Pins

Table 3.1: Pin description

PIN#	Pin name	GPIO	Stats	Function Description	Remarks
1	FORCE_USB_BOOT		I/O	Pull up to 1.8V to enter forced download mode	The pull-up source is fixed to VREG_L9A_1P8
2	NC			Reserve pins that need to remain suspended	
3	GND			GND	
4	VPH_PWR		PI	Module provides 3 VPH_PWR power pins. The voltage ranges from 3.5V to 4.2V.	External surge protection with additional capacitors and Zener diodes.
5	VPH_PWR				
6	VPH_PWR				
7	GND			GND	
8	NC			Reserve pins that need to remain suspended	
9	NC				
10	GND			GND	
11	USB_HS_DM		AI/AO	USB 2.0 differential data negative	
12	USB_HS_DP		AI/AO	USB 2.0 Differential data positive	
13	GND			GND	
14	NC			Reserve pins that need to remain suspended	
15	GND			GND	
16	USB_ID/PM6225_GPIO_9		I/O	USB ID detection signal	Default high
17	UIM2_PRESENT		I/O	UIM2 Hot Swap detection	
18	UIM2_RESET		I/O	UIM2 Reset signal	
19	UIM2_CLK		I/O	UIM2 Clock signal	
20	UIM2_DATA		I/O	UIM2 data signal	
21	VREG_L20A/VSIM2		PO	1.8V/2.95V power output for VSIM2 power supply	
22	UIM1_PRESENT		I/O	UIM1 Hot swap detection	
23	UIM1_RESET		I/O	UIM1 Reset signal	
24	UIM1_CLK		I/O	UIM1 Clock signal	
25	UIM1_DATA		I/O	UIM1 Data signal	
26	VREG_L19A/VSIM1		PO	1.8V/2.95V power output for VSIM1 power supply	
27	GND			GND	
28	VREG_L22A_2P96/VSD		PO	2.96V power output for SD card power	
29	SDC2_CLK		B	SD card clock signal	
30	SDC2_CMD		B	SD card CMD signal	
31	SDC2_DATA0		B	SD card data signal	
32	SDC2_DATA1				
33	SDC2_DATA2				
34	SDC2_DATA3				
35	SD_CARD_DET_N		I/O	SD card insertion detection	

36	GND			GND	
37	NC			Reserve pins that need to remain suspended	
38	FP_INT_N/GPIO83*	GPIO83*	I/O	Universal GPIO; Volume-keys	
39	FP_RST_N/GPIO104*	GPIO104*	I/O	Universal GPIO; HOME button	
40	GPIO85*	GPIO85*	I/O	Universal GPIO	
41	TS_I2C_SCL/GPIO7	GPIO7	I/O	Universal GPIO; TS_I2C clock signal	
42	TS_INT_N/GPIO80*	GPIO80*	I/O	Universal GPIO; TS interrupt signal	
43	TS_RST_N/GPIO86	GPIO86	I/O	Universal GPIO; TS reset signal	
44	PWM/PM6225_GPIO8	GPIO16	I/O	Universal GPIO; Screen backlight chip PWM control	
45	UART1_TX/GPIO16	GPIO16	I/O	Universal GPIO; UART1 data send	
46	UART1_RX/GPIO17*	GPIO17*	I/O	Universal GPIO; UART1 data reception	
47	UART1_CTS/GPIO14*	GPIO14*	I/O	Universal GPIO; UART1 Clear Send	
48	UART1_RFR/GPIO15	GPIO15	I/O	Universal GPIO; UART1 request sent	
49	LCD_RST_N/GPIO82	GPIO82	I/O	Universal GPIO; LCD reset signal	
50	LCD_TE/GPIO81*	GPIO81*	I/O	Universal GPIO; LCD frame sync signal	
51	GND			GND	
52	MIPI_DSI0_CLK_N		AI/AO	MIPI_DSI0 clock differential signal	
53	MIPI_DSI0_CLK_P				
54	MIPI_DSI0_LANE0_N		AI/AO	MIPI_DSI0 Data differential signal	
55	MIPI_DSI0_LANE0_P				
56	MIPI_DSI0_LANE1_N				
57	MIPI_DSI0_LANE1_P				
58	MIPI_DSI0_LANE2_N				
59	MIPI_DSI0_LANE2_P				
60	MIPI_DSI0_LANE3_N				
61	MIPI_DSI0_LANE3_P				
62	GND			GND	
63	MIPI_CSI2_CLK_N		AI/AO	MIPI_CSI2 Clock differential signal	
64	MIPI_CSI2_CLK_P				
65	MIPI_CSI2_LANE0_N		AI/AO	MIPI_CSI2 Data differential signal	
66	MIPI_CSI2_LANE0_P				
67	MIPI_CSI2_LANE1_N				
68	MIPI_CSI2_LANE1_P				
69	GND			GND	
70	MIPI_CSI0_CLK_N		AI/AO	MIPI_CSI0 clock differential signal	
71	MIPI_CSI0_CLK_P				
72	MIPI_CSI0_LANE0_N		AI/AO	MIPI_CSI0 Data differential signal	
73	MIPI_CSI0_LANE0_P				
74	GND			GND	

75	CAM_MCLK2/GPIO27*	GPIO27*	I/O	General purpose GPIO; CAM clock signal 2	
76	CAM_MCLK3/GPIO28*	GPIO28*	I/O	Universal GPIO; CAM clock signal 3	
77	GND			GND	
78	ANT_WIFI/BT		I/O	WIFI/BT antenna	
79	GND		I/O	GND	
80	CAM2_RST_N/GPIO24*	GPIO24*	I/O	Universal GPIO; CAM2 reset signal cable	
81	CAM2_PWD_N/GPIO93*	GPIO93*	I/O	Universal GPIO; CAM2 sleep signal cable	
82	CAM0_RST_N/GPIO18*	GPIO18*	I/O	Universal GPIO; CAM0 reset signal cable	
83	CAM0_PWD_N/GPIO43	GPIO43	I/O	Universal GPIO; CAM0 Sleep signal cable 1	Do not pull up externally
84	CCI_I2C_SCL0/GPIO23	GPIO23	I/O	Universal GPIO; Dedicated I2C clock signal 0, for CAM only	
85	CCI_I2C_SDA0/GPIO22	GPIO22	I/O	Universal GPIO; Dedicated I2C data signal 0, for CAM only	
86	GPIO31*	GPIO31*	I/O	Universal GPIO	
87	SNS_I2C_SCL/GPIO110	GPIO110	I/O	Universal GPIO; Dedicated SNS_I2C clock signal	
88	SNS_I2C_SDA/GPIO109*	GPIO109*	I/O	Universal GPIO; Dedicated SNS_I2C data signal	
89	DBG_UART_RX/ GPIO13*	GPIO13*	I/O	Universal GPIO; DBG_UART data reception	
90	DBG_UART_TX/GPIO12	GPIO12	I/O	Universal GPIO; DBG_UART data send	
91	KYPD_VOLP_N/PM6225_GPIO5		I/O	GPIO5 for PMU; Volume plus or minus keys	
92	PM_RESIN_N		DI	Module reset signal	
93	GND			GND	
94	ANT_TRX		I/O	Main set antenna	
95	GND			GND	
96	GPIO41	GPIO41	I/O	Universal GPIO	
97	GPIO66*	GPIO66*	I/O	Universal GPIO	
98	GPIO38	GPIO38	I/O	Universal GPIO	
99	GPIO106*	GPIO106*	I/O	Universal GPIO	
100	GPIO71*	GPIO71*	I/O	Universal GPIO	
101	CAM1_MCLK1/GPIO21	GPIO21	I/O	Universal GPIO; CAM1 clock signal cable	
102	GPIO42	GPIO42	I/O	Universal GPIO	
103	GPIO45	GPIO45	I/O	Universal GPIO	External pull-ups prohibited
104	GPIO40	GPIO40	I/O	Universal GPIO	
105	Board_ID/GPIO49	GPIO49	I/O	Universal GPIO; Board_ID detection signal	
106	ALSP_INT_N/GPIO35*	GPIO35*	I/O	Universal GPIO; Dedicated optical pitch sense interrupt signal	

107	MAG_INT_N/GPIO34*	GPIO34*	I/O	Universal GPIO; Dedicated geomagnetic interrupt signal	
108	GYRO_INT/GPIO33*	GPIO33*	I/O	Universal GPIO; Dedicated gyroscope interrupt signal	
109	ACCEL_INT/GPIO32*	GPIO32*	I/O	Universal GPIO; Dedicated accelerometer interrupt signal	
110	LPI_MI2S2_CLK/GPIO102*	GPIO102*	I/O	Universal GPIO; LPI_MI2S2 clock signal	
111	LPI_MI2S2_WS/GPIO103*	GPIO103*	I/O	Universal GPIO; LPI_MI2S2 slice selector signal	
112	GPIO52	GPIO52	I/O	Universal GPIO	
113	SPI_SCLK/GPIO2	GPIO2	I/O	Universal GPIO; SPI clock signal	
114	SPI_CSN/GPIO3*	GPIO3*	I/O	Universal GPIO; SPI slice selector signal	
115	SPI_MISO/GPIO0*	GPIO0*	I/O	Universal GPIO; SPI main input from output	
116	SPI_MOSI/GPIO1	GPIO1	I/O	Universal GPIO; SPI main output from input	
117	GPIO84*	GPIO84*	I/O	Universal GPIO	
118	GPIO97*	GPIO97*	I/O	Universal GPIO	
119	GND			GND	
120	ANT_GPS		I/O	GPS antenna	
121	GND			GND	
122	VREG_L7P_1P8		PO	1.8V power output	For CAM IO power supply
123	KYPD_PWR_N		DI	Switching machine	Internal 1.8V pull-up, low active.
124	NC			Reserve pins that need to remain suspended	
125	NC				
126	VCOIN		AI/AO	External backup battery provides power to system real-time clock when system power supply VPH_PWR is absent. The backup battery is charged when VPH_PWR is present.	3. Connect a 3V button battery or large capacitor to the VCOIN pin.
127	NC			Reserve pins that need to remain suspended	
128	ADC/PM6225_GPIO3	GPIO3	I/O	GPIO3 for PMU; ADC input detection	
129	VREG_L9A_1P8		PO	1.8V power output	The system is normally powered for signal pull-up or sensor IO power supply.
130	VREG_CAM0_AVDD_2P8		PO	2.8V power output for CAM0_AVDD power supply	
131	GND			GND	
132	ANT_DRX		I/O	Diversity antenna	
133	GND			GND	

134	EAR_OUT_P		AO	Receiver output positive	
135	EAR_OUT_M		AO	Receiver output negative	
136	GND			GND	
137	CDC_HPH_R		AO	Right track of headphones	
138	CDC_HPH_REF		AI	Headphone reference place	
139	CDC_HPH_L		AO	Left track of headphones	
140	CDC_HS_DET		DI	Earphone unplug detection	
141	MIC2_IN_N		AI	MIC2 differential input negative	The MIC bias circuit has been connected internally
142	MIC2_IN_P		AI	MIC2 Differential input positive	
143	GND			GND	
144	MIC1_N		AI	MIC1 differential input negative	The MIC bias circuit has been connected internally
145	MIC1_P		AI	MIC1 Differential input positive	
146	GND			GND	
147	WCD_AUX_OUT_M		AO	AUX output negative	Class AB output, need to connect audio PA
148	WCD_AUX_OUT_P		AO	AUX output positive	
149	GND			GND	
150	TS_I2C_SDA/GPIO6*	GPIO6*	I/O	Universal GPIO; TS_I2C data signal	
151	NC			Reserve pins that need to remain suspended	
152	GND			GND	
153	GND				
154	GND				
155	GND				
156	GND				
157	GND				
158	TS_I2C_SDA/GPIO6*		I/O	Universal GPIO; TS_I2C data signal	
159	NC			Reserve pins that need to remain suspended	
160	GND			GND	
161	GND				
162	GND				
163	GND				
164	GND				
165	CBL_PWR_N		DI	Power on automatic power on signal	Connect the 1K resistance to the ground and power on the automatic power on.
166	NC			Reserve pins that need to remain suspended	
167	NC				
168	USB_IN_DET		DI	USB interrupt detection signal	
169	NC			Reserve pins that need to remain suspended	
170	GND			GND	
171	GND				

172	USB_SS_TX0_P		AI/AO	USB 3.1 Differential Data Channel 0	
173	USB_SS_RX0_P				
174	USB_SS_TX0_M				
175	USB_SS_RX0_M				
176	GND			GND	
177	GND				
178	GND				
179	MIPI_CSI2_LANE3_N		AI/AO	MIPI_CSI2 Data differential signal	
180	MIPI_CSI2_LANE3_P				
181	MIPI_CSI2_LANE2_P				
182	GND			GND	
183	MIPI_CSI2_LANE2_N		AI/AO	MIPI_CSI2 Data differential signal	
184	MIPI_CSI0_LANE1_P		AI/AO	MIPI_CSI0 Data differential signal	
185	MIPI_CSI0_LANE1_N				
186	MIPI_CSI0_LANE2_P				
187	MIPI_CSI0_LANE2_N				
188	MIPI_CSI0_LANE3_P				
189	MIPI_CSI0_LANE3_N				
190	GND			GND	
191	GND				
192	NC			Reserve pins that need to remain suspended	
193	NC				
194	NC				
195	NC				
196	GND			GND	
197	GND				
198	NC			Reserve pins that need to remain suspended	
199	NC				
200	NC				
201	NC				
202	NC				
203	NC				
204	GND			GND	
205	GND				
206	CCI_I2C_SCL1/GPIO30	GPIO30	I/O	Universal GPIO; Dedicated I2C clock signal 1, for CAM only	
207	UART2_RX/GPIO70*	GPIO70*	I/O	Universal GPIO	No UART function
208	CCI_I2C_SDA1/GPIO29	GPIO29	I/O	Universal GPIO; Dedicated I2C data signal 1, for CAM only	
209	UART2_TX/GPIO69*	GPIO69*	I/O	Universal GPIO	No UART function
210	GPIO36*	GPIO36*	I/O	Universal GPIO	
211	GPIO96*	GPIO96*	I/O	Universal GPIO	
212	GPIO39*	GPIO39*	I/O	Universal GPIO	
213	CAM0_MCLK0/GPIO20	GPIO20	I/O	General purpose GPIO; CAM0 clock signal cable	
214	CAM1_RST_N/GPIO19*	GPIO19*	I/O	Universal GPIO; CAM1 Reset signal cable	

215	CAM0_PWD_N/GPIO68	GPIO68	I/O	Universal GPIO; CAM0 Sleep signal cable 2	
216	CAM3_RST_N/GPIO65*	GPIO65*	I/O	Universal GPIO; CAM3 reset signal cable	
217	CAM1_PWD_N/GPIO46*	GPIO46*	I/O	Universal GPIO; CAM1 sleep signal cable	Do not pull up externally
218	GPIO111	GPIO111	I/O	Universal GPIO	
219	MI2S_MCLK1/GPIO108	GPIO108	I/O	Universal GPIO; MI2S clock signal 1	
220	GPIO112*	GPIO112*	I/O	Universal GPIO	
221	MI2S_MCLK2/GPIO107*	GPIO107*	I/O	Universal GPIO; MI2S clock signal 2	
222	VREG_CAM1_AVDD_2P8		PO	2.8V power output for CAM1_DVDD power supply	
223	NC			Reserve pins and keep them suspended	
224	VREG_CAM_AF_2P8		PO	2.8V power output for CAM_AF power supply	
225	NC			Reserve pins that need to remain suspended	
226	VREG_CAM0_DVDD_1P104		PO	1.104V power output for CAM0_DVDD power supply	Adjustable 1.2V output
227	NC			Reserve pins that need to remain suspended	
228	GND			GND	
229	GND				
230	GND				
231	GND				
232	GND				
233	MIC3_IN_N		AI	MIC3 differential input negative	The MIC bias circuit has been connected internally
234	MIC_BIAS1		AO	MIC bias voltage	
235	GND			GND	
236	GND				
237	GND				
238	MI2S1_WS/GPIO99*	GPIO99*	I/O	Universal GPIO; MI2S1 slice selector signal	It can be configured as DMIC1_DATA
239	MI2S1_DATA0/GPIO100	GPIO100	I/O	Universal GPIO; MI2S1 data signal 0	Configurable as DMIC2_CLK
240	MI2S1_DATA1/GPIO101	GPIO101	I/O	Universal GPIO; MI2S1 Data Signal 1	Can be configured as DMIC2_DATA
241	VREG_L15A_3P128		PO	3.128V Power Output	For USB-related circuits
242	NC			Reserve pins that need to remain suspended	
243	ADC/PM6225_GPIO6		I/O	GPIO6 for PMU; ADC input detection	
244	MIC3_IN_P		AI	MIC3 Differential input positive	The MIC bias circuit has been connected internally
245	PM6225_GPIO2	GPIO2	I/O	GPIO2 at PMU	
246	GND			GND	

247	MI2S1_CLK/GPIO98	GPIO98	I/O	Universal GPIO; MI2S1 clock signal	Can be configured to DMIC1_CLK
248	NC			Reserve pins that need to remain suspended	
249	GPIO47	GPIO47	I/O	Universal GPIO	
250	GND			GND	
251	MI2S_MCLK0/GPIO105*	GPIO105*	I/O	Universal GPIO; MI2S clock signal 0	Can be configured as LPI_MI2S2_DATA 1
252	NC			Reserve pins that need to remain suspended	
253	GND			GND	
254	USB_SS_RX1_M		AI/AO	USB3.1 Differential Data Channel 1	
255	USB_SS_TX1_M				
256	MIPI_CSI1_CLK_N		AI/AO	MIPI_CSI1 Clock differential signal	
257	MIPI_CSI1_CLK_P				
258	MIPI_CSI1_LANE0_N		AI/AO	MIPI_CSI1 Data differential signal	
259	MIPI_CSI1_LANE1_N				
260	MIPI_CSI1_LANE2_N				
261	MIPI_CSI1_LANE3_N				
262	MIPI_CSI1_LANE3_P				
263	NC			Reserve pins that need to remain suspended	
264	VREG_ CAM1_DVDD _1P2		PO	1.2V power output for CAM1_DVDD power supply	
265	VREG_L6P_3P0		PO	3.0V power output	For sensor power supply
266	VREG_L6P_3P0				
267	APPS_I2C_SDA/GPIO4*	GPIO4*	I/O	APPS_I2C data signal	It can only be configured as I2C and has been pulled up internally
268	APPS_I2C_SCL/ GPIO5	GPIO5	I/O	APPS_I2C clock signal	
269	USB_SS_RX1_P		AI/AO	USB3.1 Differential Data Channel 1	
270	USB_SS_TX1_P				
271	MIPI_CSI1_LANE0_P		AI/AO	MIPI_CSI1 Data differential signal	
272	MIPI_CSI1_LANE1_P				
273	MIPI_CSI1_LANE2_P				
274	NC			Reserve pins that need to remain suspended	
275	GND			GND	
276	USB_PHY_PS		I/O	USB PHY port selection	Connect the 1K resistor to the ground, the default is Micro USB mode

Note: GPIO with * supports interrupt function

3.3. Mechanical Dimensions

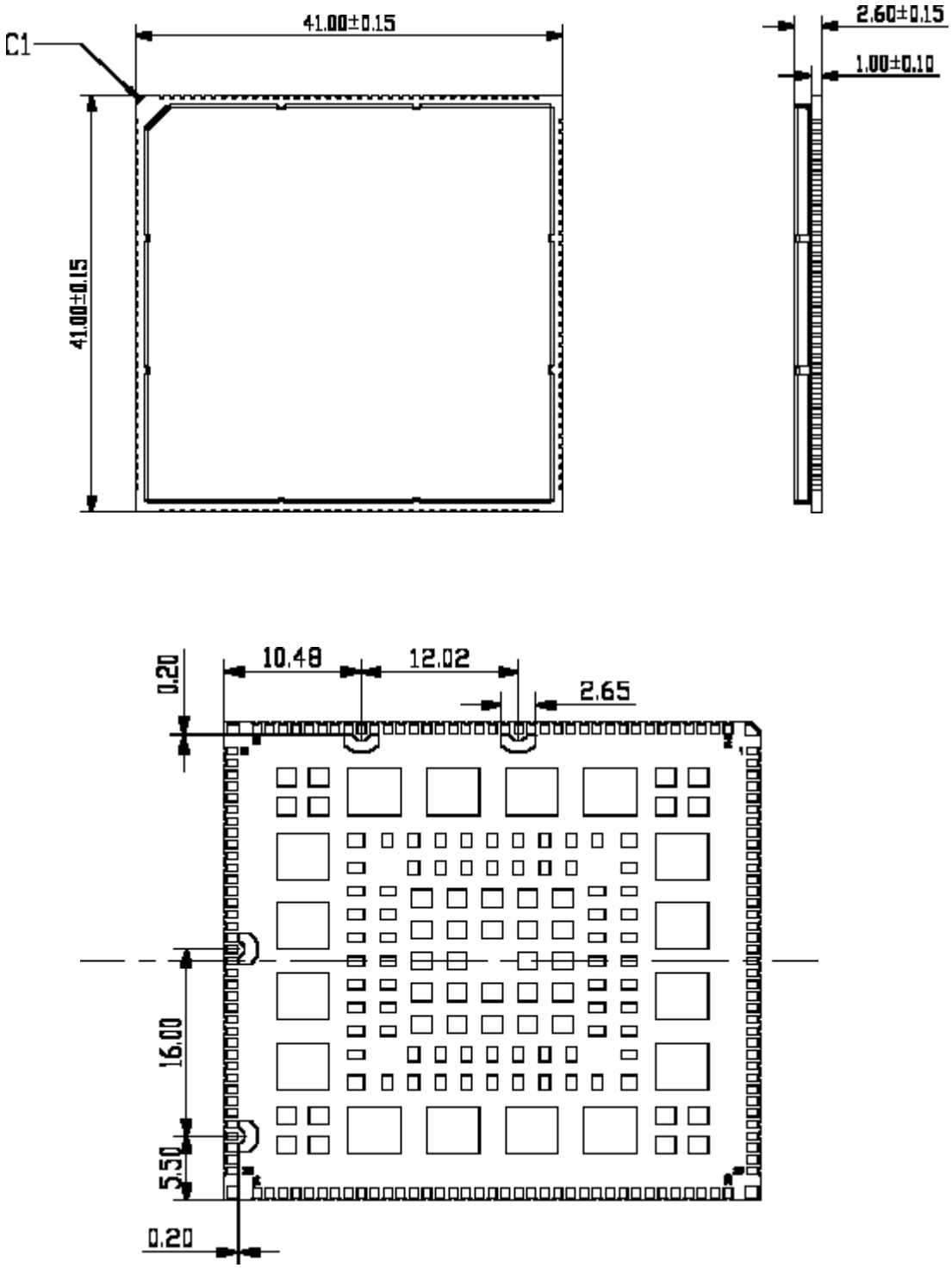


Figure 3.2: Three-dimensional dimensions of the module (unit: mm)

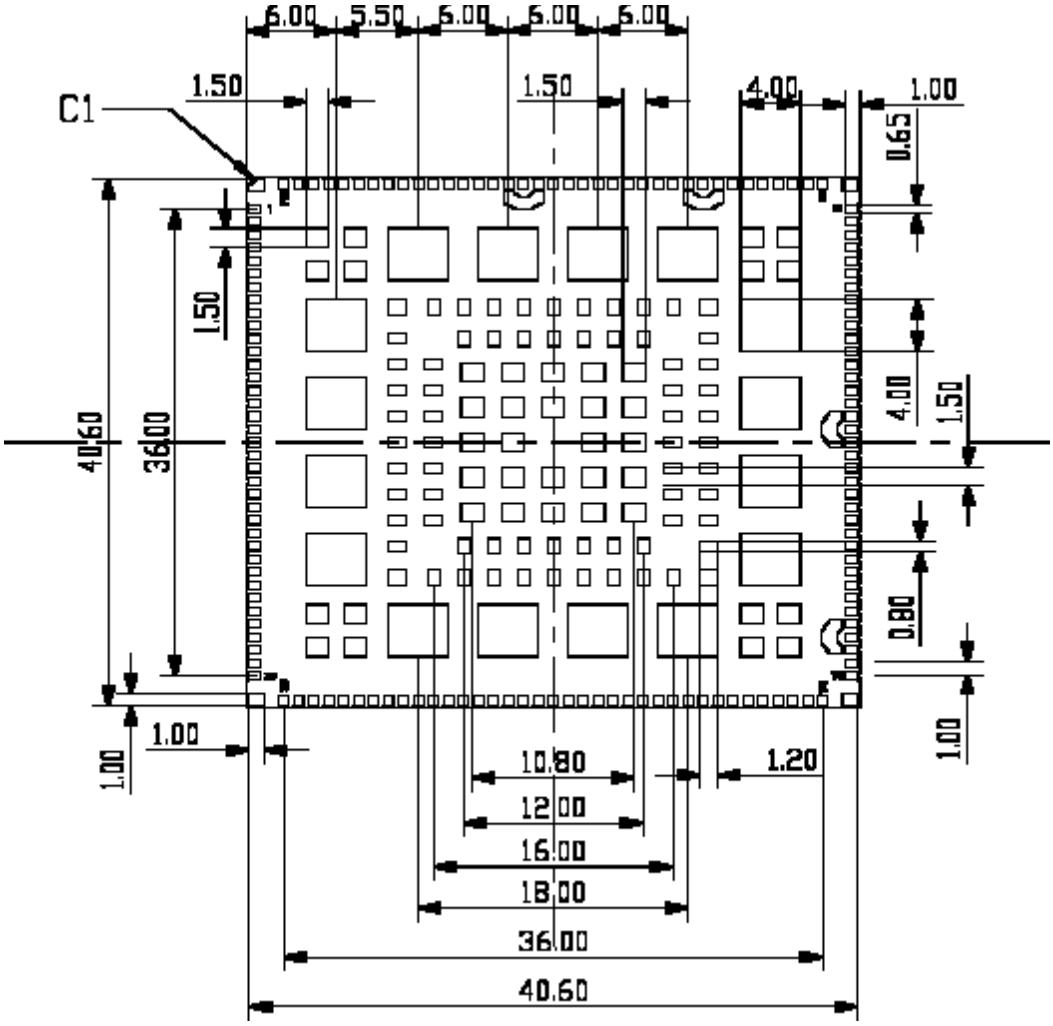


Figure 3.3: Recommended package (unit: mm)

4. Interface application

4.1. Power Supply

If it is a battery device, the voltage input range of the module VPH_PWR is 3.5V to 4.2V, and the recommended voltage is 3.8V. In the GSM band, when the module is transmitted at maximum power, the peak current can reach up to 3A in an instant, resulting in a large voltage drop on the VPH_PWR.

It is recommended to use a large capacitor to regulate the voltage near the VPH_PWR. It is recommended to use 2 47uF ceramic capacitors, and parallel 33PF and 10PF capacitors can effectively remove high-frequency interference. At the same time, in order to prevent ESD and surge damage to the chip, it is recommended to use a suitable TVS tube and 5.1V/500mW Zener diode in the module VPH_PWR pin. PCB layout, capacitor and diode should be as close as possible to the module VPH_PWR pin. The user can directly power the module with a 3.8V lithium-ion battery, and when using the battery, the impedance between the VPH_PWR pin and the battery should be less than 150mΩ.

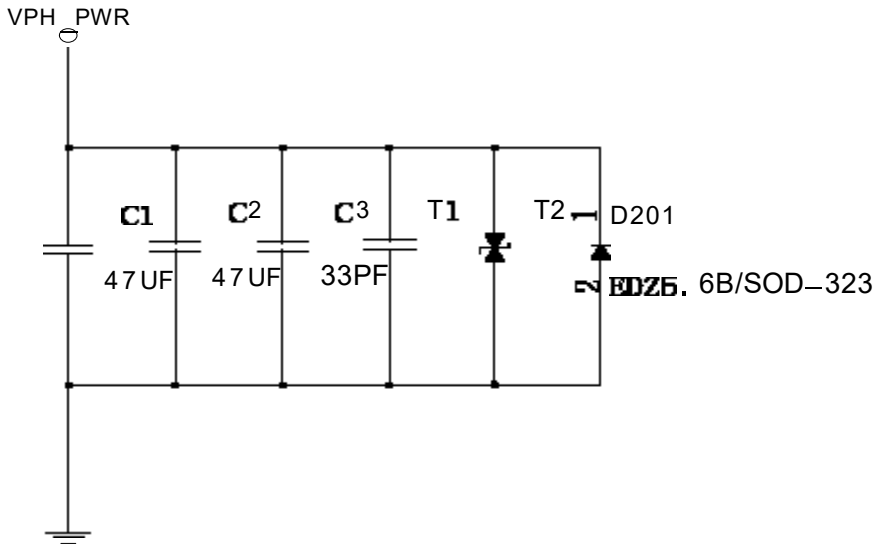


Figure 4.1: VPH_PWR input reference circuit

If it is a DC-powered device and the DC input voltage is 5V-12V, the recommended circuit that can use DC-DC power is shown below:

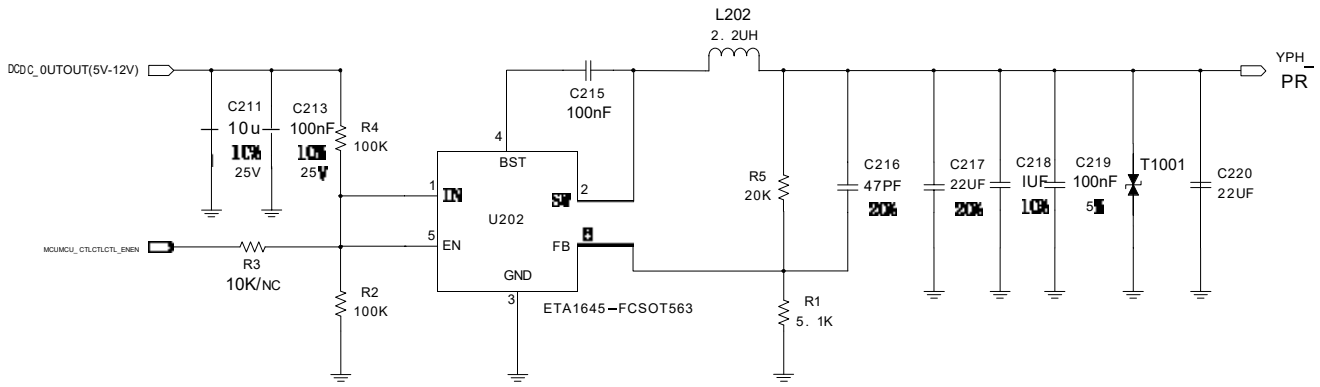


Figure 4.2: DC-DC powered reference circuit

4.1.1. Power Supply Pins

VPH_PWR pins (4, 5, 6) are used for power input. In the user's design, please pay special attention to the design of the power supply part to ensure that the drop of VPH_PWR is not lower than 3.5V even when the module power consumption reaches 3A. If the voltage drop is lower than 3.5V, the module may shut down. The PCB wiring from the VPH_PWR pin to the power supply should be wide and short enough to reduce voltage drop in transmission burst mode.

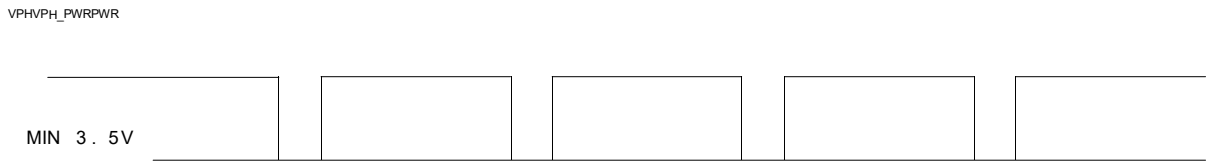


Figure 4.3: VPH_PWR drop minimum voltage

4.1.2. PCB Layout of Power Supply

The power routing should not only consider VPH_PWR, but also the return GND of the power supply. The VPH_PWR positive line must be short and thick, and the line must first pass through the large capacitor, Zener diode and then to the power PIN of the module. There are multiple PAD exposed copper at the bottom of the module, and it is necessary to ensure that the GND path from these exposed copper areas to the power supply is the shortest and most unobtainable. In this way, the current path of the entire power supply can be ensured to be shortest, and the interference can be minimal.

4.2. Power on and Off

Do not turn on the module when it exceeds the normal operating temperature and voltage upper limits of the module. In extreme cases such operation can cause permanent damage to the module.

4.2.1. Power-on of the Module

The user can start the module by pulling down the KYPD_PWR_N pin (123) for at least 2 seconds. This pin has been pulled up to the 1.8V power supply in the module. The recommended circuit is as follows;

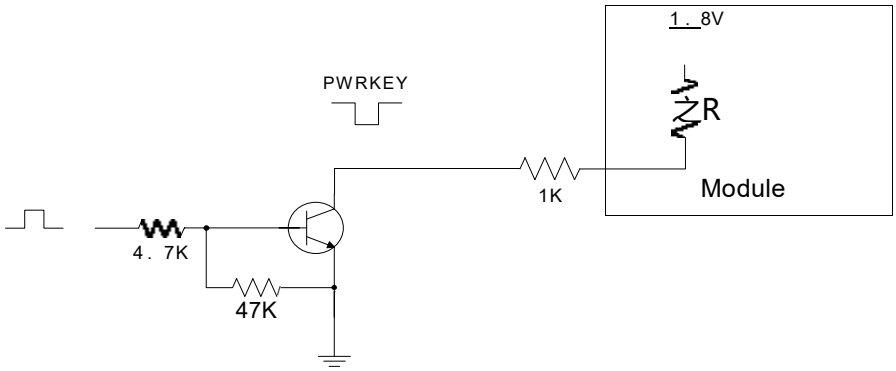


Figure 4.4: External signal drive module power-on reference design

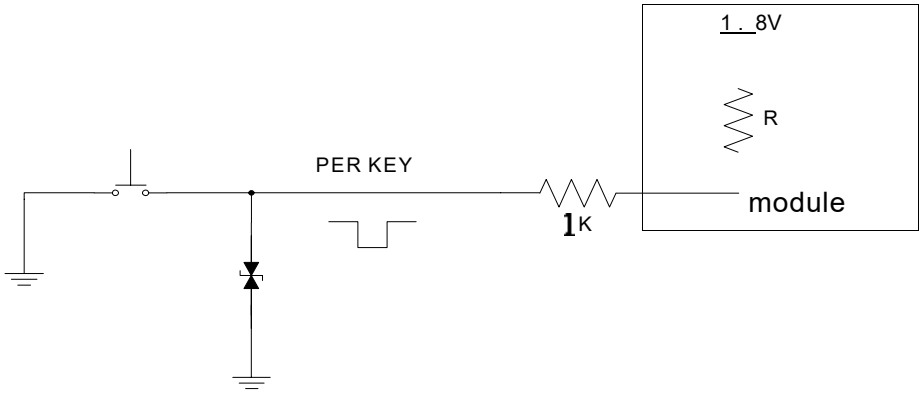


Figure 4.5: push-button power-on reference circuit

Below is the power-on timing instruction:

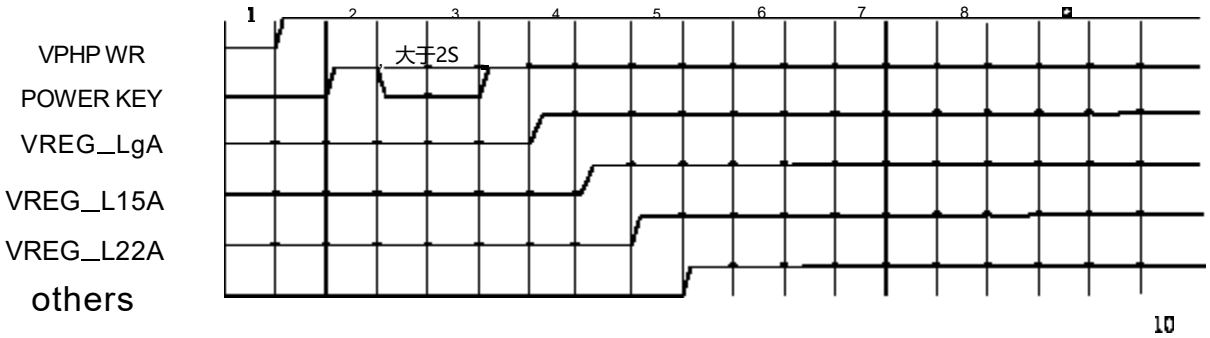


Figure 4.6: PWRKEY power on timing diagram

4.2.2. Module Shutdown

The user can power off by long pressing the KYPD_PWR_N pin

4.2.2.1. KYPD_PWR_N Shutdown

Users can shut down the KYPD_PWR_N signal by pulling it down for at least 3 seconds. The shutdown circuit can refer to the design of the power on circuit. After the module detects the shutdown action, a prompt window will pop up on the screen to confirm whether to execute the shutdown action.

The user can force shutdown by holding down KYPD_PWR_N for a long time, at least 12 seconds.

4.2.3. Module Reset

The SLM927 module supports the hardware reset function, and the user can quickly restart the module by pulling down the PM_RESIN_N (92) pin of the module. The recommended circuit is as follows:

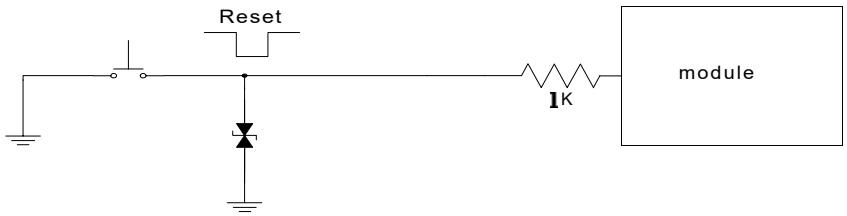


Figure 4.7: Reference design of key reset circuit

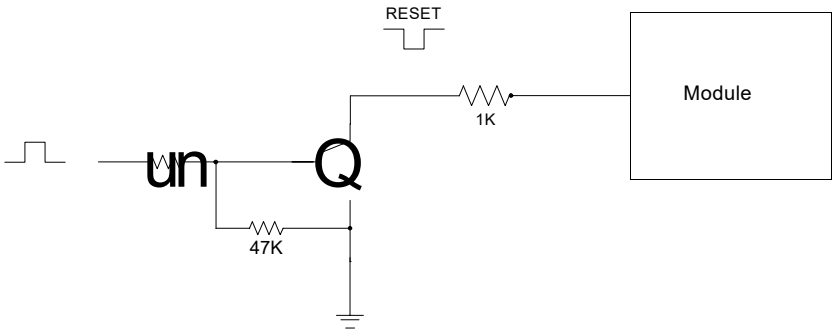


Figure 4.8: Reference design of external signal reset circuit

The typical value of the normal voltage of the pin is 1.8V, so the user with the level of 3V or 3.3V can not directly use the MCU GPIO to drive the pin, and need to add the isolation circuit. The hardware parameters of PM_RESIN_N can refer to the following table:

Table 4.1: Hardware parameters of PM_RESIN_N

PIN	Description	Minimum	Typical value	Maximum value	Units
PM_RESIN_N	Input high level	1.4	1.8	-	V
	Input low level	-	0	0.6	V
	Pull down the effective time	500		-	ms

4.3. RTC Power Supply

When the VPH_PWR is disconnected, the user needs to save the real-time clock, then the VCOIN (126) pin can not be suspended, should be connected with a large capacitor or button battery, when the external capacitor is connected, the recommended value is 100uF. When the VCOIN power supply uses the external large capacitor or battery to power the RTC inside the module, the reference design circuit is as follows:

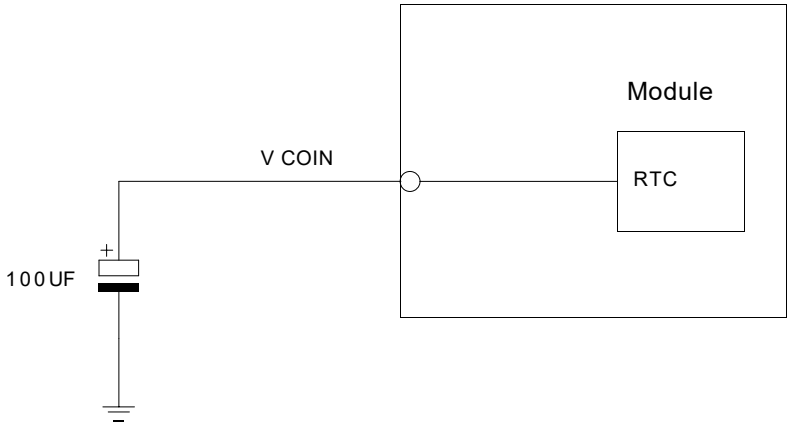


Figure 4.9: External capacitor power supply circuit to RTC

Rechargeable battery power supply:

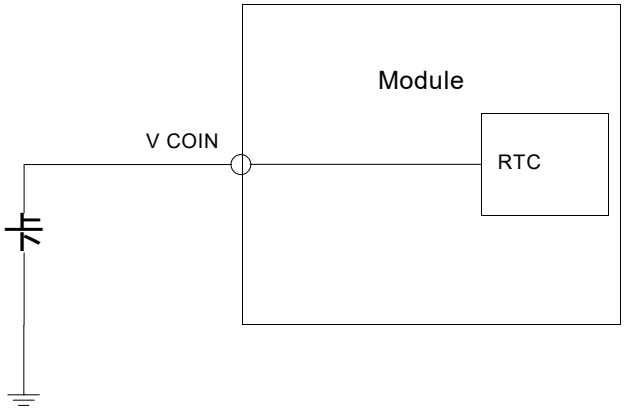


Figure 4.10: Rechargeable battery feeds RTC power circuit

VCOIN power supply typically has a value of 3.0V.

4.4. Power Output

The SLM927 has multiple power outputs. For peripherals pull up, CAM, sensor, touch panel, etc. In the application, it is recommended to add parallel 33PF and 10PF capacitors in each power supply can effectively remove high-frequency interference.

Table 4.2: Power supply description

Signals	Default voltage (V)	Maximum output current (mA)
VREG_L20A	1.8	100

VREG_L22A_2P96/VSD	2.96	600
VREG_L7P_1P8	1.8	300
VREG_L9A_1P8	1.8	150
VREG_CAM0_AVDD_2P8	2.8	300
VREG_CAM1_AVDD_2P8	2.8	300
VREG_CAM_AF_2P8	2.8	300
VREG_CAM0_DVDD_1P104	1.104	300
VREG_L15A_3P128	3.128	100
VREG_ CAM1_DVDD _1P2	1.2	300
VREG_L6P_3P0	1.8	300

4.5. Serial Port

The SLM927 provides two UART interfaces for communication. The UART1 supports hardware flow control. The number of UART interfaces can be increased through QUP interface function reuse.

Table 4.3: UART pin description

Name	Pins	Directions	Features
UART1_TX/GPIO16	45	I/O	UART1 Data sending
UART1_RX/GPIO17*	46	I/O	UART1 Data reception
UART1_CTS/GPIO14*	47	I/O	UART1 Clear Send
UART1_RFR/GPIO15	48	I/O	UART1 Request sent
DBG_UART_TX/GPIO12	90	I/O	DBG_UART data sending
DBG_UART_RX/ GPIO13*	89	I/O	DBG_UART Data receiving

You can refer to the following figure to connect:

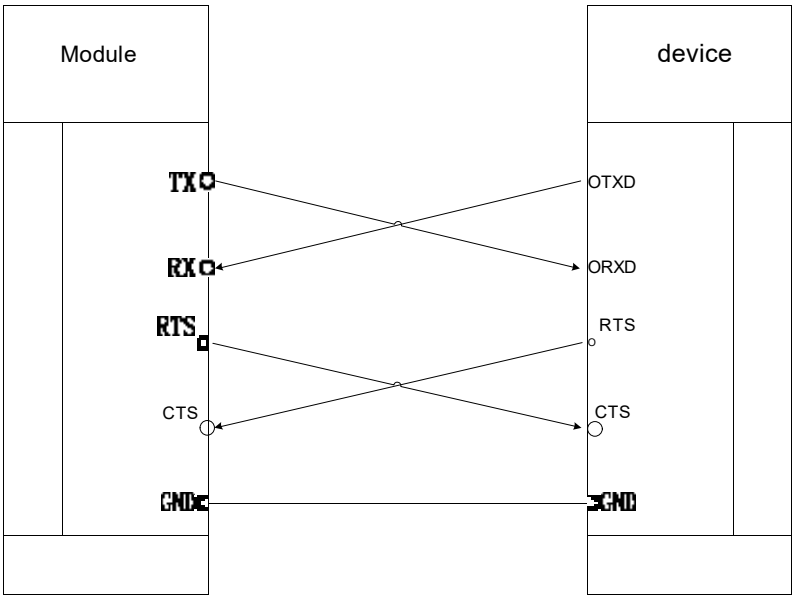


Figure 4.11: Serial port connection diagram

When the level of the serial port used by the user does not match the module, in addition to adding the level conversion IC, the following figure can also be used to achieve level matching, here only the matching circuit on TX and RX is listed, other low speed signals can refer to these two circuits.

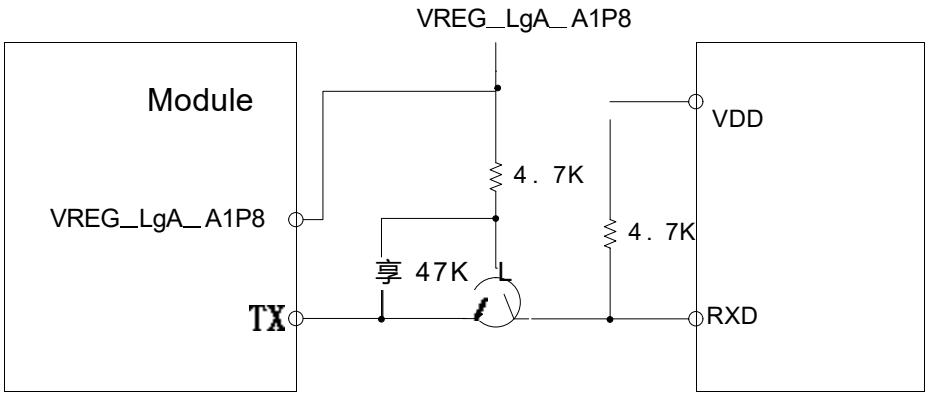


Figure 4.12: Schematic diagram of TX level switching

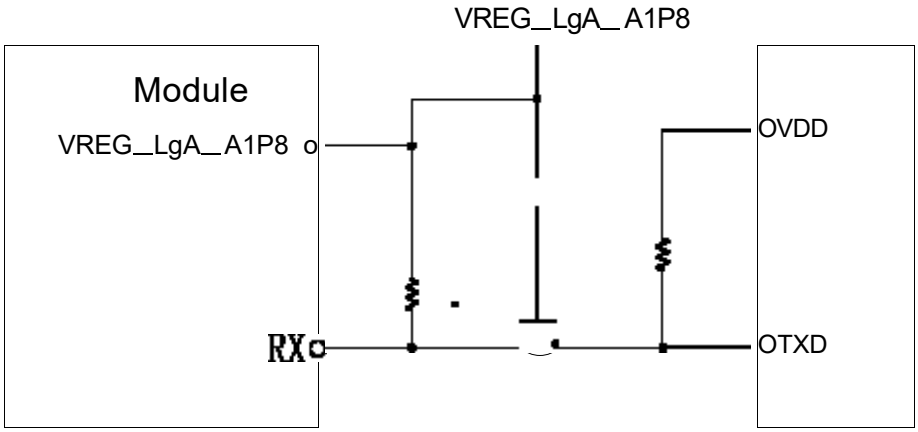


Figure 4.13：Schematic diagram of RX level conversion

Table 4.4: Serial port hardware parameters

Description	Minimum	Maximum	Units
Input low	-	0.63	V
Enter high	1.17	-	V
Output low	-	0.45	V
Output high	1.35	-	V

Note: 1. The serial port of the module is CMOS interface and cannot be directly connected to RS232 signal. If required, use an RS232 conversion chip.

2. If the 1.8V output of the module cannot meet the high level range of the client, ask the user to add a level conversion circuit.

4.6. MIPI Interface

The SLM927 supports the MIPI interface for Camera and LCD. MIPI is a high-speed signal line, in the Layout stage, please strictly follow the impedance, length requirements of the line, control the difference pair within the group, the group equal length, the total length as short as possible.

4.6.1. LCD Interface

The SLM927 module supports one set of MIPI interfaces for the LCD. The resolution of the screen can be supported up to FHD+(2520X1080)@90Hz. In Layout, MIPI signal line please strictly control the difference 85±10% ohm impedance control and signal line within and between groups equal length.

The MIPI interface of the module is 1.2V voltage domain. When the user needs to design compatible screen, the ADC pin or GPIO of the module can be used as LCM_ID. The module does not provide the power required by the display screen, please use LDO for external power supply.

Table 4.5: Screen interface definition

Screen Interface			
MIPI_DSI0_CLK_N	52	AI/AO	MIPI_DSI0 clock differential signal
MIPI_DSI0_CLK_P	53	AI/AO	
MIPI_DSI0_LANE0_N	54	AI/AO	MIPI_DSI0 Data differential signal
MIPI_DSI0_LANE0_P	55	AI/AO	
MIPI_DSI0_LANE1_N	56	AI/AO	
MIPI_DSI0_LANE1_P	57	AI/AO	
MIPI_DSI0_LANE2_N	58	AI/AO	
MIPI_DSI0_LANE2_P	59	AI/AO	
MIPI_DSI0_LANE3_N	60	AI/AO	
MIPI_DSI0_LANE3_P	61	AI/AO	
LCD_RST_N/GPIO82	49	I/O	Universal GPIO; LCD reset signal
LCD_TE/GPIO81*	50	I/O	Universal GPIO; LCD frame sync signal
PWM/PM6225_GPIO8	44	I/O	Universal GPIO; Screen backlight chip PWM control

MIPI is a high-speed signal line, in order to avoid EMI interference with the radio frequency, the common mode inductor is placed near the LCD side as needed.

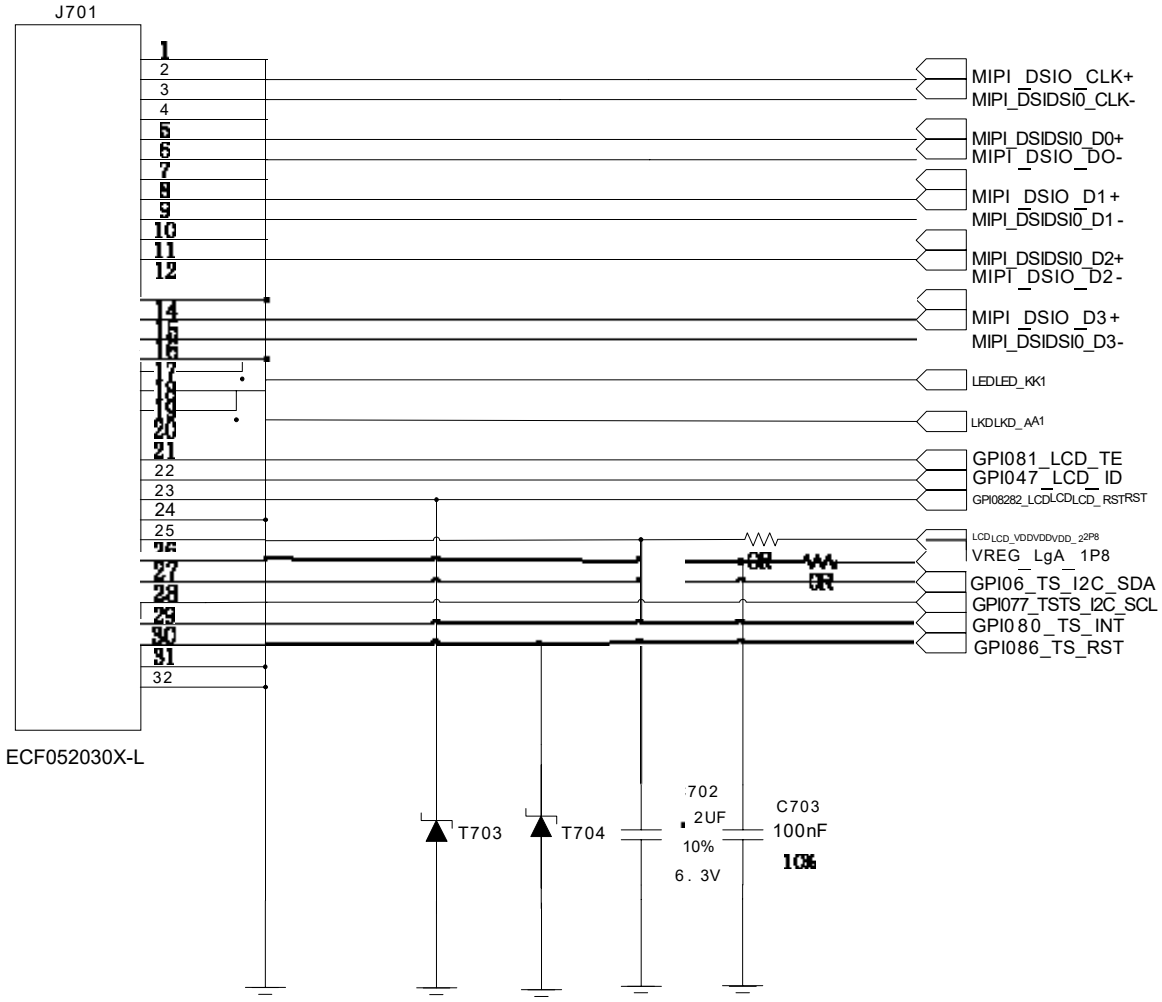


Figure 4.14: Screen interface reference circuit

SLM927 does not support backlight driver output, customers need to use an external backlight driver. The backlight driver circuit can be referred to Figure 4.15. The brightness of backlight can be adjusted through PWM/PM6225_GPIO8 (44) of the module, and the modulation mode is PWM mode.

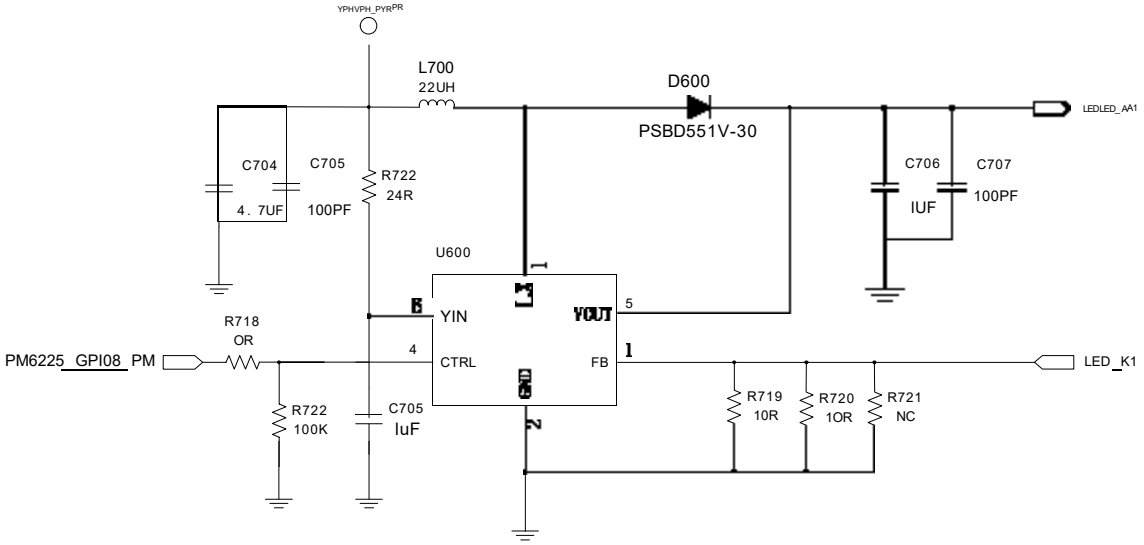


FIG. 4.15: External backlight circuit diagram

Note: The user should select the correct driver chip based on the backlight circuit of the LCD. The reference circuit

provided in this document is the series PWM dimming backlight driver circuit; If it is a series type one-line dimming type backlight driver circuit, it needs to be controlled by GPIO.

4.6.2. Camera Interface

SLM927 supports 3 groups of MIPI-CSI interfaces. Support 13MP+13MP+5MP at 30fps ZSL triple shot design, support 25MP+5MP or 16M+16M at 30fps ZSL dual shot design, support 32MP at 30fps ZSL single shot design.

Table 4.6: MIPI-CSI interface definition

CSI0 interface			
Name	Pins	Input/Output	Description
MIPI_CSI0_CLK_N	70	AI/AO	MIPI_CSI0 clock differential signal
MIPI_CSI0_CLK_P	71	AI/AO	
MIPI_CSI0_LANE0_N	72	AI/AO	MIPI_CSI0 Data differential signal
MIPI_CSI0_LANE0_P	73	AI/AO	
MIPI_CSI0_LANE1_N	185	AI/AO	
MIPI_CSI0_LANE1_P	184	AI/AO	
MIPI_CSI0_LANE2_N	187	AI/AO	
MIPI_CSI0_LANE2_P	186	AI/AO	
MIPI_CSI0_LANE3_N	189	AI/AO	
MIPI_CSI0_LANE3_P	188	AI/AO	
CAM0_MCLK0/GPIO20	213	I/O	General purpose GPIO; CAM0 clock signal
CAM0_RST_N/GPIO18*	82	I/O	Universal GPIO; CAM0 reset signal cable
CAM0_PWD_N/GPIO43	83	I/O	Universal GPIO; CAM0 sleep signal cable
CCI_I2C_SDA0/GPIO22	85	I/O	Dedicated CAM I2C0
CCI_I2C_SCL0/GPIO23	84	I/O	
VREG_CAM0_AVDD_2P8	130	PO	2.8V power output for CAM0_AVDD power
VREG_CAM0_DVDD_1P104	226	PO	1.104V power output for CAM0_DVDD power supply
VREG_CAM_AF_2P8	224	PO	2.8V power output for CAM_AF power supply

CSI2 interface			
Name	Pins	Input/Output	Description
MIPI_CSI2_CLK_P	64	AI/AO	MIPI_CSI2 Clock differential signal
MIPI_CSI2_CLK_N	63	AI/AO	
MIPI_CSI2_LANE0_P	66	AI/AO	MIPI_CSI2 Data differential signal
MIPI_CSI2_LANE0_N	65	AI/AO	
MIPI_CSI2_LANE1_P	68	AI/AO	
MIPI_CSI2_LANE1_N	67	AI/AO	
MIPI_CSI2_LANE2_P	181	AI/AO	
MIPI_CSI2_LANE2_N	183	AI/AO	
MIPI_CSI2_LANE3_P	180	AI/AO	

MIPI_CSI2_LANE3_N	179	AI/AO	
CAM2_RST_N/GPIO24*	80	I/O	Universal GPIO; CAM2 reset signal cable
CAM2_PWD_N/GPIO93*	81	I/O	Universal GPIO; CAM2 sleep signal cable
CAM_MCLK2/GPIO27*	75	I/O	Universal GPIO; CAM2 clock signal
CCI_I2C_SCL1/GPIO30	206	I/O	Dedicated CAM I2C1
CCI_I2C_SDA1/GPIO29	208	I/O	
VREG_CAM1_AVDD_2P8	222	PO	2.8V power output for CAM1_AVDD power
VREG_CAM_AF_2P8	224	PO	2.8V power output for CAM_AF power supply
VREG_ CAM1_DVDD_1P2	264	PO	1.2V power output for CAM1_DVDD power

CSI1 Interface			
Name	Pins	Input/Output	Description
MIPI_CSI1_CLK_N	256	AI/AO	MIPI_CSI1 Clock differential signal
MIPI_CSI1_CLK_P	257	AI/AO	
MIPI_CSI1_LANE0_N	258	AI/AO	MIPI_CSI1 Data differential signal
MIPI_CSI1_LANE0_P	271	AI/AO	
MIPI_CSI1_LANE1_N	259	AI/AO	
MIPI_CSI1_LANE1_P	272	AI/AO	
MIPI_CSI1_LANE2_N	260	AI/AO	
MIPI_CSI1_LANE2_P	273	AI/AO	
MIPI_CSI1_LANE3_N	261	AI/AO	
MIPI_CSI1_LANE3_P	262	AI/AO	
CAM1_MCLK1/GPIO21	101	I/O	Universal GPIO; CAM1 clock signal cable
CAM1_RST_N/GPIO19*	214	I/O	Universal GPIO; CAM1 Reset signal cable
CAM1_PWD_N/GPIO46*	217	I/O	General purpose GPIO; CAM1 sleep signal
CCI_I2C_SCL1/GPIO30	206	I/O	Dedicated CAM I2C1
CCI_I2C_SDA1/GPIO29	208	I/O	
VREG_CAM1_AVDD_2P8	222	PO	2.8V power output for CAM1_AVDD power
VREG_ CAM1_DVDD_1P2	264	PO	1.2V power output for CAM1_DVDD power supply

If the user designs a CAMERA module with autofocus function, please note that the I2C of the module cannot be directly connected to the AF device; the I2C of the AF device should be connected to the driver chip of the CAMERA.

MIPI interface rate is high, the user in the wiring stage, please press 85±10% ohm impedance control, at the same time, please pay attention to the requirements of the length of the line, do not increase the small capacitance on the MIPI signal line, which may affect the MIPI data rising edge time, and then lead to the MIPI data invalid.

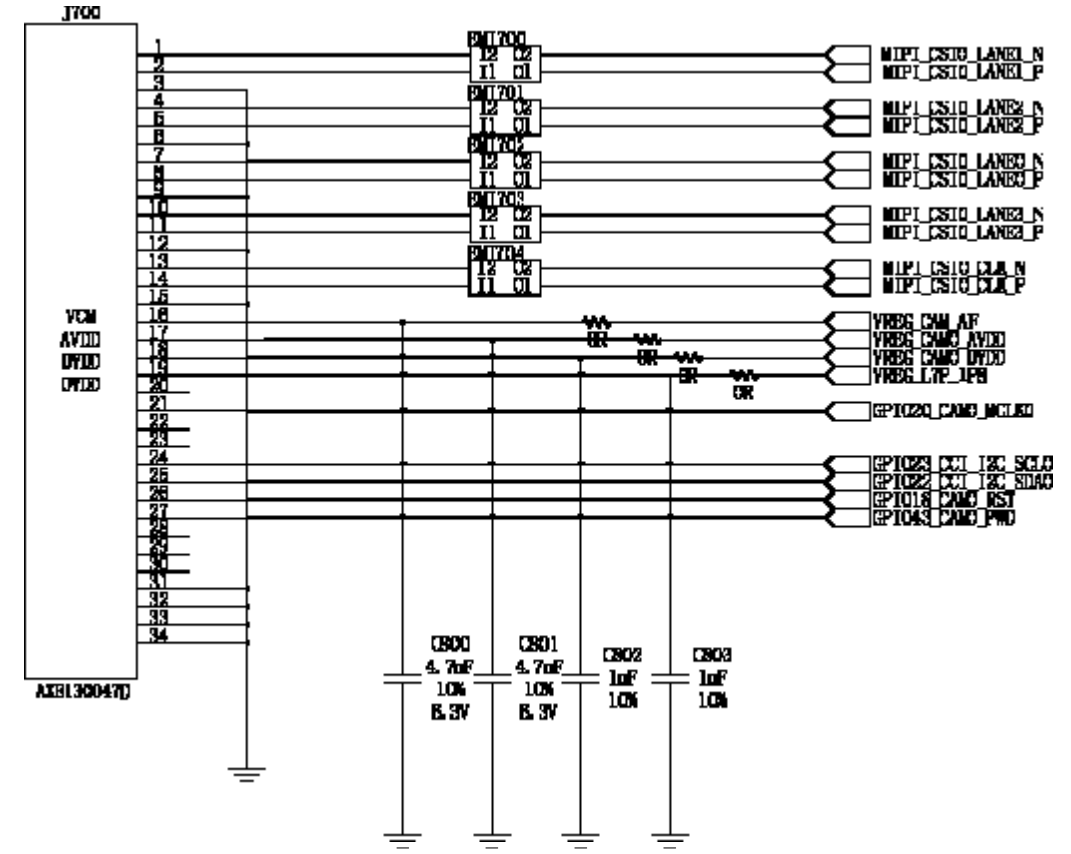


Figure 4.16: MIPI Camera (CIS0) reference circuit

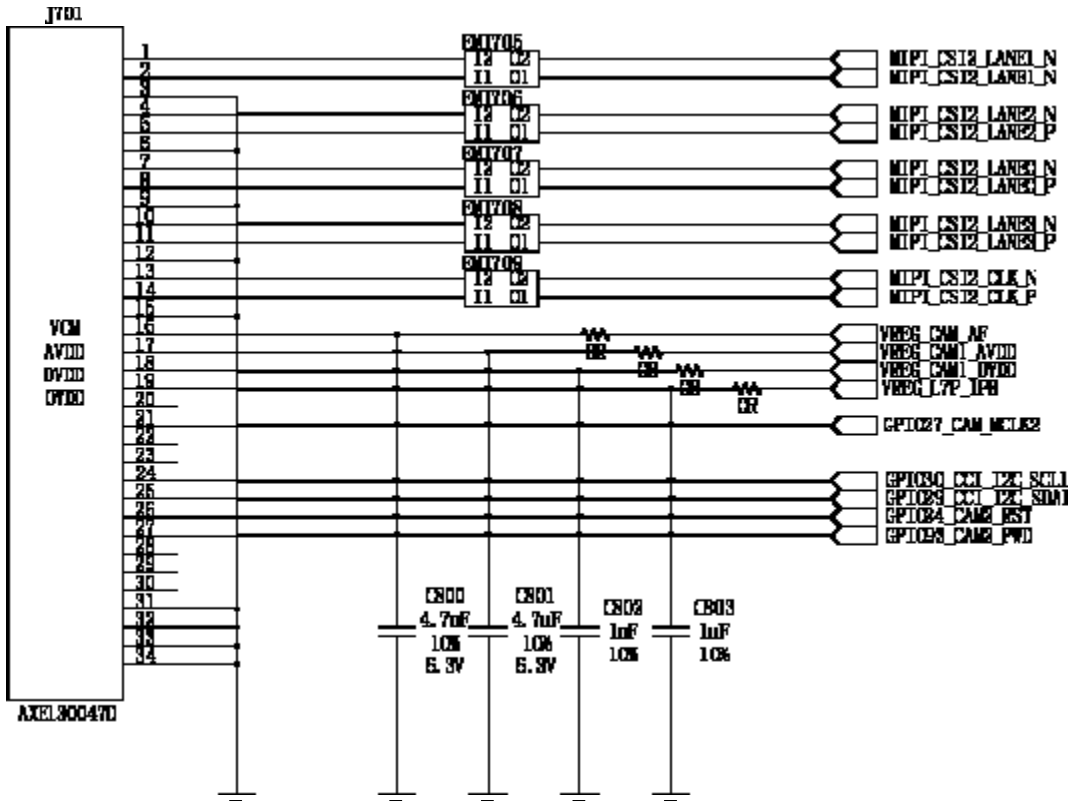


Figure 4.17: MIPI Camera(CSI2) reference circuit

4.6.3. MIPI PCB Layout

MIPI is a high-speed signal line, the user must pay attention to protection in the layout stage, so that it is far away from the signal line that is easy to be interfered with. It must be treated with GND on the upper and lower sides, and the wiring is in the way of differential pairs. 85±10% ohm differential impedance matching is done.

MIPI interface in the selection of ESD devices, please select a small capacitance value of TVS, it is recommended that the parasitic capacitance is less than 1pF.

MIPI cable requirements are as follows:

- The total cable length should not exceed 150mm.
- It is required to control 85 ohm differential impedance, error ±10%.
- The difference line length error in the group is controlled within 0.7mm.
- The length error between groups is controlled within 1.4mm.

4.7. Capacitive Touch Interface

Module provides a set of I2C interface can be used to connect capacitive touch, while providing the required power supply and interrupt pins, capacitive touch software default interface pins defined as follows:

Table 4.7: Capacitive touch interface definition

Name	lead	Input/Output	Description
TS_I2C_SCL/GPIO7	41	I/O	I2C signal with 2.2K resistance pull-up to VREG_L9A_1P8
TS_I2C_SDA/GPIO6*	150/158	I/O	
TS_INT_N/GPIO80*	42	I/O	Universal GPIO; TS interrupt signal
TS_RST_N/GPIO86	43	I/O	Universal GPIO; TS reset signal

Note: The interface definition of capacitive touch can be adjusted by software, and the user can change the GPIO and I2C according to the design needs.

4.8. Audio Interface

The module provides three analog audio inputs, MIC1_ P/N is used to connect the main microphone; MIC2_IN_P/N can be used to connect the headset mike, and MIC3_IN_P/M can be used to connect the noise-cancelling mike. The three mics are already connected to the bias circuit inside the module. At the same time, the module provides three analog audio outputs (CDC_HPH_L/R, EAR_OUT_P/M, WCD_AUX_OUT_P/M). The audio pin pin is defined as follows:

Table 4.8: Audio pin pin definition

Name	Pins	Input/Out	Description
MIC1_N	144	AI	MIC1 differential input negative
MIC1_P	145	AI	MIC1 Differential input positive
MIC2_IN_N	141	AI	MIC2 differential input negative
MIC2_IN_P	142	AI	MIC2 Differential input positive
MIC3_IN_N	233	AI	MIC3 differential input negative

MIC3_IN_P	244	AI	MIC3 Differential input positive
MIC_BIAS1	234	AO	MIC bias voltage
CDC_HPH_R	137	AO	Right track of headphones
CDC_HPH_L	139	AO	Left track of headphones
CDC_HS_DET	140	AI	Headset unplug detection
CDC_HPH_REF	138	AI	Headphone reference place
EAR_OUT_M	135	AO	Receiver output negative
EAR_OUT_P	134	AO	Receiver output positive
WCD_AUX_OUT_M	147	AO	AUX output negative
WCD_AUX_OUT_P	148	AO	AUX output positive

Note: It is recommended that users choose the following circuit according to the actual application situation, in order to get a better sound effect.

4.8.1. Receiver Interface Circuit

The receiver interface circuit places the following devices near the receiver end, B302 and B303 can be changed to magnetic beads according to the actual effect.

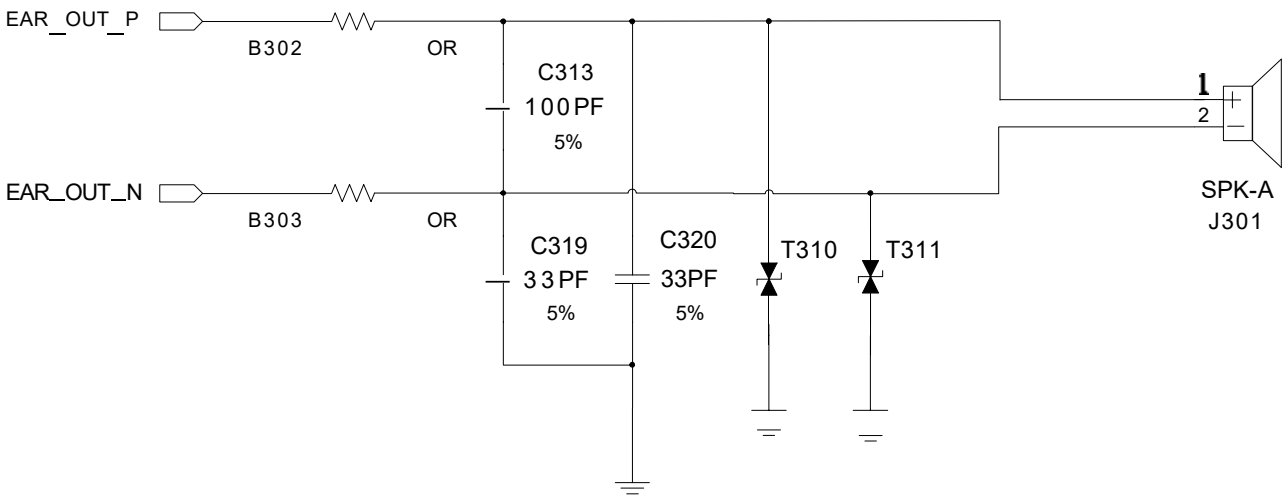


Figure 4.18: Receiver reference circuit

4.8.2. Microphone Receiving Circuit

Below are the electret microphone (ECM) reference circuit and analog Silicon microphone (MEMS) reference circuit respectively.

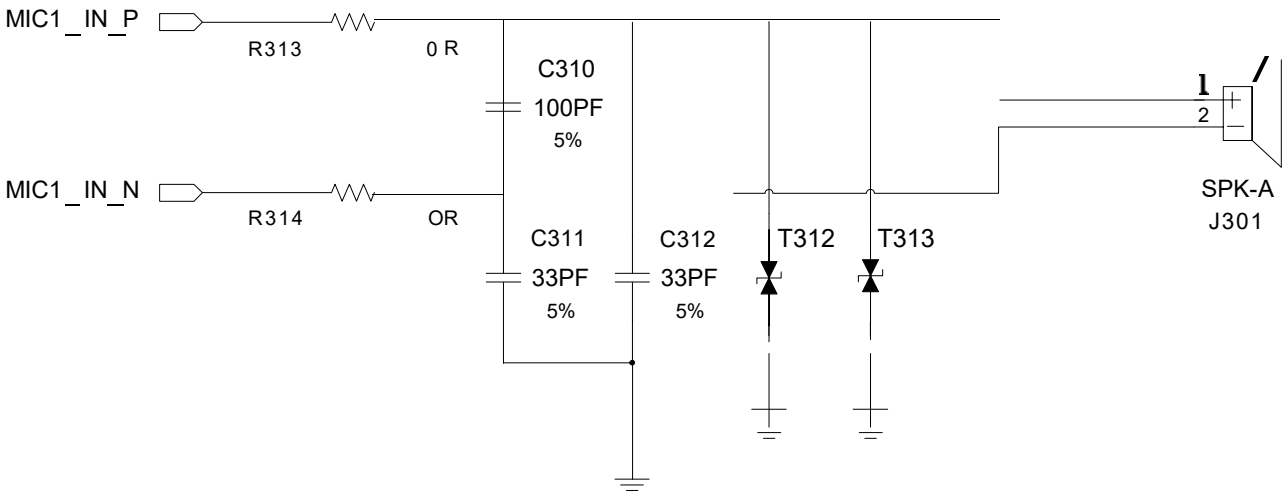


Figure 4.19: Electret microphone reference circuit

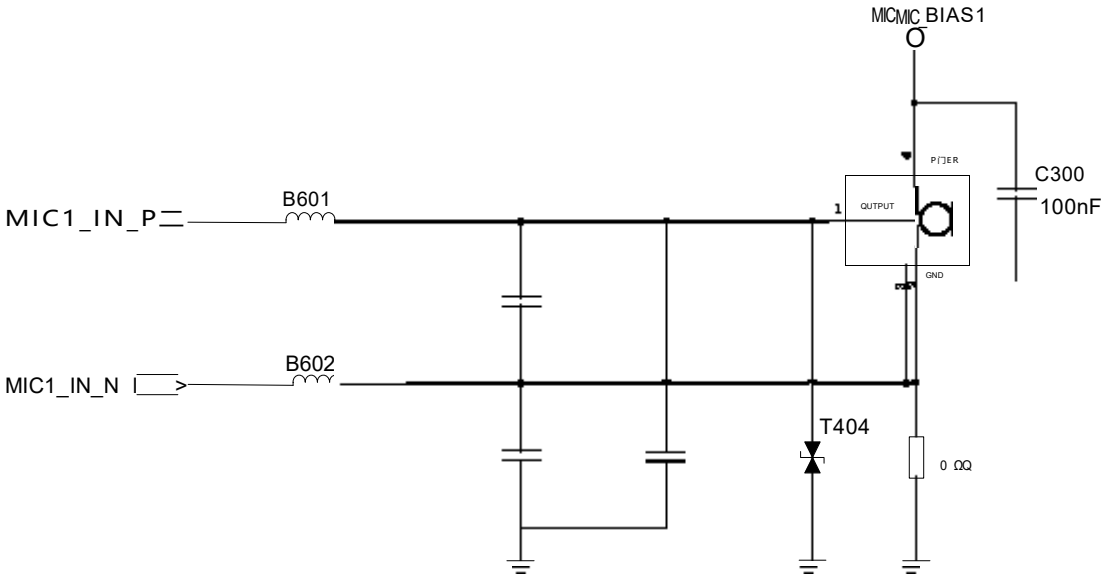


Figure 4.20: Silicon microphone reference circuit

4.8.3. Headphone Jack Circuit

The module integrates one stereo headphone jack. It is recommended to reserve ESD devices during the design phase to prevent ESD damage. The CDC_HS_DET pin of the module can be set to interrupt, and the default pin in the software is the earphone interrupt, and the user can realize the plug and remove detection of the earphone through the pin.

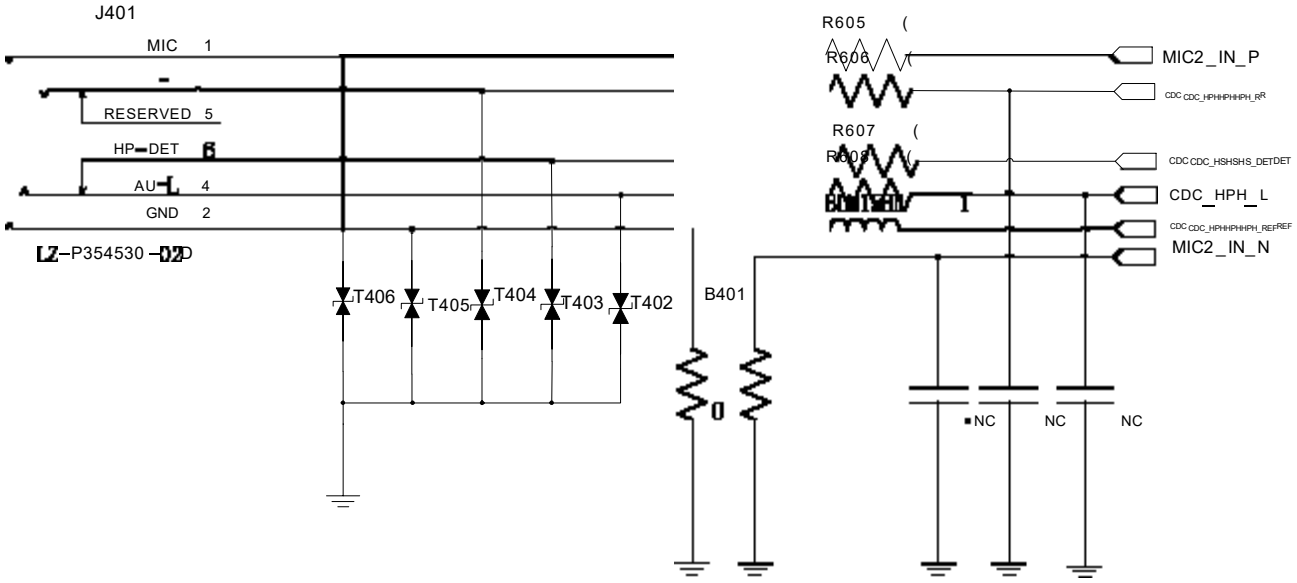


Figure 4.21: Headphone jack circuit

Note:

1. The earphone holder in Figure 4.21 is normally closed. If the user uses the earphone holder in normally open mode, please modify the detection circuit according to the actual pin and modify the software accordingly.

2. We recommend that CDC_HS_DET and CDC_HPH_L form a detection circuit (the connection mode in the figure above), because CDC_HPH_Lhas a pull-down resistance inside the chip, which can ensure that CDC_HS_DET and CDC_HPH_L are low when connected. If the user connects CDC_HS_DET with CDC_HPH_R, please reserve the position of 1K pulldown resistance on CDC_HPH_R.

3 The standard of the headphone interface shown in the figure is CTIA. If you need to design the OMTP interface, you need to swap the GND and MIC signals for the network. If you want to be compatible with both headphone standards, you need to connect an external dedicated chip, such as TI-TS3A226AE.

4.8.4. Speaker Interface Circuit

The WCD_AUX_OUT_M/P output of the module requires external audio PA to drive the speaker effectively. The reference circuit is shown in the image below.

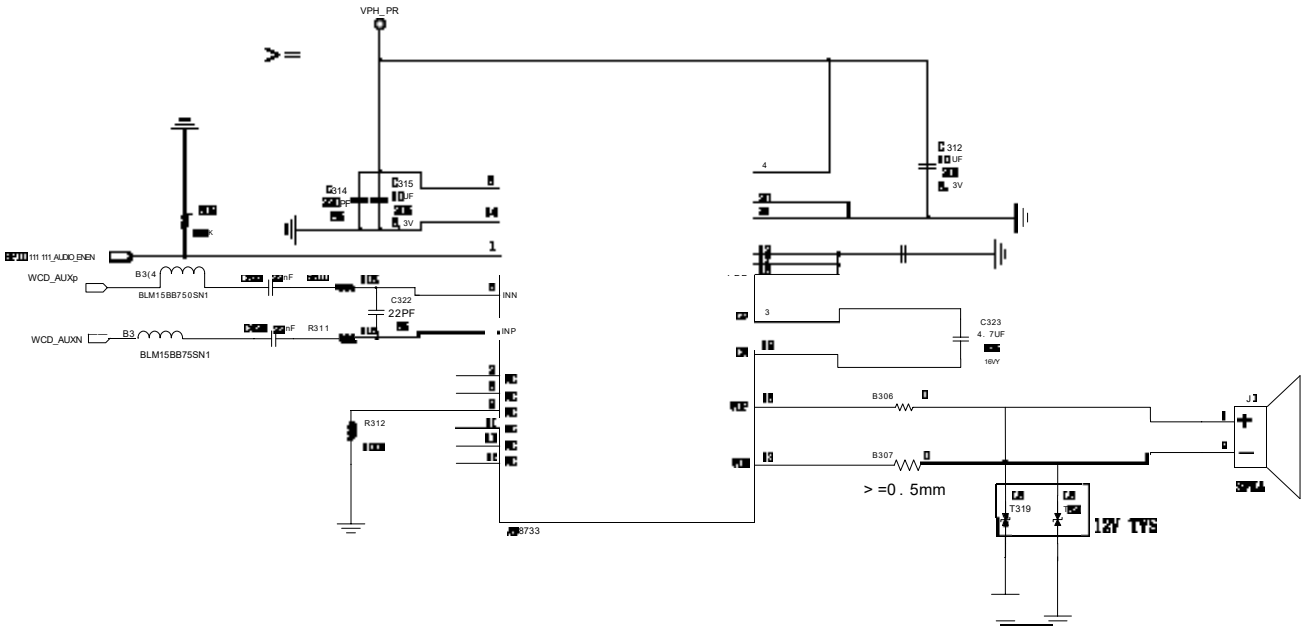


Figure 4.22: External audio power amplifier reference circuit

4.8.5. I2S Interface

The module supports one set of I2S interfaces by default. If the user needs two sets of I2S, the second set of I2S can be reused through a specific GPIO.

Table 4.9: I2Spin pin definition

Name	Pins	Input/Output	Description
MI2S1_DATA0/GPIO100	239	I/O	General purpose GPIO; MI2S1 data signal
MI2S1_DATA1/GPIO101	240	I/O	
MI2S1_WS/GPIO99*	238	I/O	Universal GPIO; MI2S1 frame
MI2S1_CLK/GPIO98	247	I/O	Universal GPIO; MI2S1 bit clock
MI2S_MCLK0/GPIO105*	251	I/O	Universal GPIO MI2S master clock

The group of I2S can also be multiplexed into DMIC signals, as shown in Table 3-1

4.8.6. AUDIO PCB Layout

Analog signals are susceptible to interference from high speed digital signals and power supplies. So stay away from high speed digital signal lines and power supply lines. The module supports GSM standard, and the GSM signal can interfere with the audio through coupling and conduction. The user can add 33pF and 10pF capacitors to the audio channel to filter out the coupling interference. The 33pF capacitor mainly filters out interference in the GSM850/EGSM900 band, and the 10pF capacitor mainly filters out interference in the DCS1800 band. The coupling interference of TDD has a lot to do with the user's PCB design. In some cases, the TDD of GSM850/EGSM900 band is more serious, and in some cases, the TDD interference of DCS1800 band is more serious. Therefore, the user can choose the required filter capacitor according to the actual test results, and sometimes there is no need to paste filter capacitor.

GSM antenna is the main source of TDD coupling interference, so users should pay attention to the audio routing away from GSM antenna and VPH_PWR when PCB layout and wiring. It is best to place a group of filter capacitors near the module end, and another group near the interface end. The audio output should be routed according to the differential

signal rules.

The conducted interference is mainly caused by the voltage drop of VPH_PWR, if the Audio PAis directly powered by VPH_PWR, it is easier to hear the "squeak" sound at the SPK output end, so it is best to parallel some large capacity capacitors and series magnetic beads at the input end of the Audio PAin the schematic design. TDD and GND also have a great relationship, if the GND is not handled well, many high-frequency interference signals will interfere with the MIC and Speaker through bypass capacitors and other devices, so the user should ensure the good performance of GND in the PCB design stage.

4.9. USB Interface

The SLM927 supports one USB 3.1 port and one USB2.0 port. Be sure to control 90±10% ohm differential impedance when Layout, and control the external cable length.

The module supports OTG function at the same time, but the user needs to add DCDC to provide OTG power.

SLM927 module does not support the charging function, and USB_IN_DET only has the function ofUSB plug and plug detection. The USB interface pins are as follows:

Table 4.10: USB pin definitions

Name	Pins	Input/Output	Description
USB_SS_RX1_P	269	AI/AO	USB 3.1 Differential Data Channel 1
USB_SS_RX1_M	254	AI/AO	
USB_SS_TX1_P	270	AI/AO	
USB_SS_TX1_M	255	AI/AO	
USB_SS_RX0_P	173	AI/AO	USB 3.1 Differential Data Channel 0
USB_SS_RX0_M	175	AI/AO	
USB_SS_TX0_P	172	AI/AO	
USB_SS_TX0_M	174	AI/AO	
USB_HS_DP	12	AI/AO	usb
USB_HS_DM	11	AI/AO	

Table 4.11: USB_IN_DET voltage input range

name	Description	Minimum	Typical	Max	Units
USB_IN_DET	Enter range	3.6	5	10	V

The USB plug and unplug detection of the module is realized by USB_IN_DET, when the USB cable is inserted, the voltage of USB_IN_DET will trigger the interrupt inside the module, so if the user needs to use the USB function, please be sure to connect the USB_IN_DET to the 5V power supply on the data cable.

USB is in high speed mode, it is recommended to connect the common mode inductor in series near the USB connector side, which can effectively suppress EMI interference. At the same time, the USB interface is an external interface, which can increase the TVS tube and strengthen the electrostatic protection. When choosing TVS, please note that the load capacitance should be less than 1pf. USB_IN_DET also needs to increase the TVS tube, if there is a surge prevention demand, but also increase the surge prevention tube. The connection diagram is as follows:

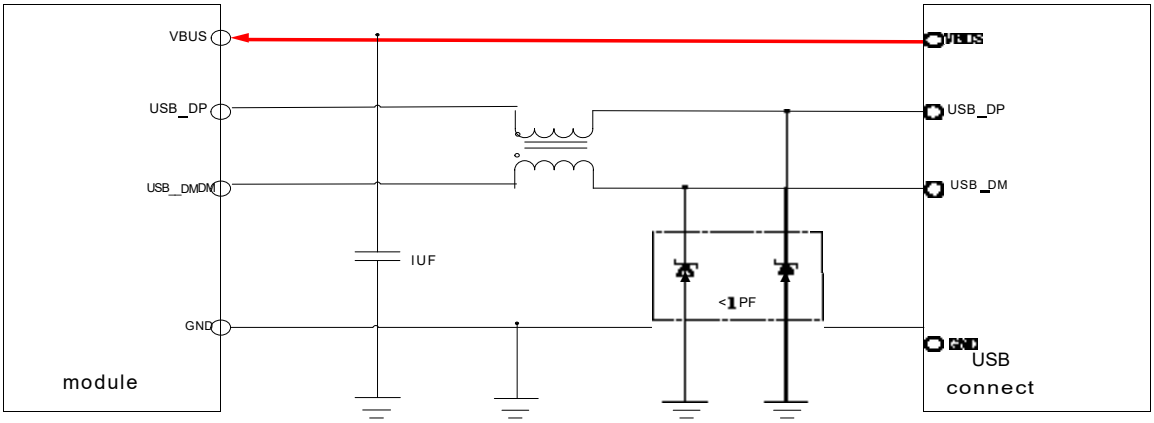


Figure 4.23: USB connection diagram

4.9.1. USB OTG

The SLM927 module can provide USB OTG function, but the OTG power supply requires the customer's external circuit. The pins used for this function are listed below:

Table 4.12: USB OTGpin description

Pin Names	Pins	Description
USB_HS_DM	11	USB 2.0 differential data negative
USB_HS_DP	12	USB 2.0 Differential data positive
USB_ID/PM6225_GPIO_9	16	USB_ID
USB_IN_DET	168	USB interrupt detection signal

4.9.2. USB PCB Layout

The user suggests adding a common mode inductor in the schematic design stage, which can effectively suppress EMI interference. If the user needs to increase electrostatic protection, please be sure to select TVS tubes with parasitic capacitance less than 1pF.

In the Layout, please refer to the following precautions:

The common mode inductor should be near the side of the USB connector;

It is required to control 90 ohm differential impedance, error ±10%;

USB2.0 difference line internal length error control within 2mm;

USB3.1 difference line internal length error control within 0.7mm;

If there is a test point, try to avoid the cable bifurcation, the test point is placed on the path of the cable.

Table 4.13: USB cable lengths inside the module

Pins	Signals	Length (mm)	Length error (P-N)
12	USB_HS_DP	31.84	0.03
11	USB_HS_DM	31.87	
172	USB_SS_TX0_P	19.49	0.02
174	USB_SS_TX0_M	19.47	

173	USB_SS_RX0_P	15.15	0
175	USB_SS_RX0_M	15.15	
270	USB_SS_TX1_P	15.11	0
255	USB_SS_TX1_M	15.11	
269	USB_SS_RX1_P	16.21	0
254	USB_SS_RX1_M	16.21	

4.10. (U)SIM Card Interface

4.10.1. UIM Card Interface Circuit

SLM927 can support two (U)SIM card interfaces at the same time to achieve dual SIM card dual standby. It supports hot swappable (U)SIM cards and can automatically identify 1.8V and 3.0V cards. Below is the (U)SIM recommended interface circuit. In order to protect the (U)SIM card, it is recommended to use TVS device for electrostatic protection. The device of the peripheral circuit of the (U)SIM card should be near the (U)SIM card seat.

The reference circuit is as follows:

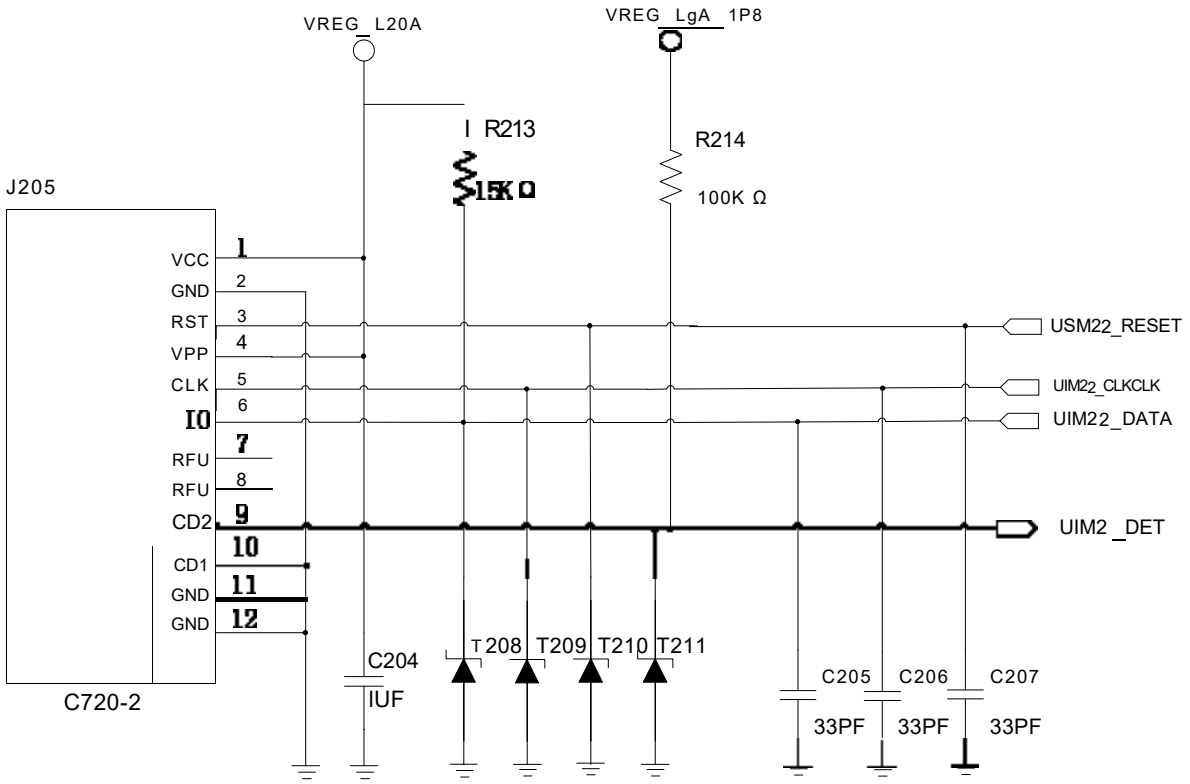


Figure 4.24: UIM2 card interface circuit

4.10.2. UIM PCB Layout

The SIM card area is large, and there is no anti-EMI interference device itself, it is easy to be interfered with, so in the layout, first ensure that the SIM card is far away from the antenna and the antenna extension line inside the product, as close as possible to the module, pay attention to the protection of SIM_CLK signal when the PCB is running.

SIM_DATA, SIM_RST and SIM_CLK signals of the SIM card should be far away from the power supply and away from the high-speed signal line. If it is not handled well, it is easy to cause the situation of not recognizing the card or dropping the card, so please follow the following principles when designing:

In the PCB layout stage must be the SIM card seat away from the GSM antenna;

SIM card cable should be as far away from RF line, VPH_PWR and high-speed signal line as possible, while SIM card cable should not be too long;

The GND of the SIM card seat should maintain good connectivity with that of the module, so that the GND of the two is equal potential;

To prevent SIM_CLK from interfering with other signals, it is recommended that SIM_CLKbe protected.

It is recommended to place a 100nF capacitor near the SIM card seat on the SIM_VDD signal line;

TVS is placed near the SIM card seat, the parasitic capacitance of the TVS should not be greater than 50pF, and the 51Ω resistance in series between the module can enhance ESD protection;

Add 22pfground capacitance to the SIM card signal line to prevent RF interference;

The backflow path of the VPH_PWR has a high current. Therefore, avoid the backflow path of the VPH_PWR when routing SIM cards.

4.11. SD Card Interface

The SLM927 supports an SD card interface up to 256GB

The reference circuit is as follows:

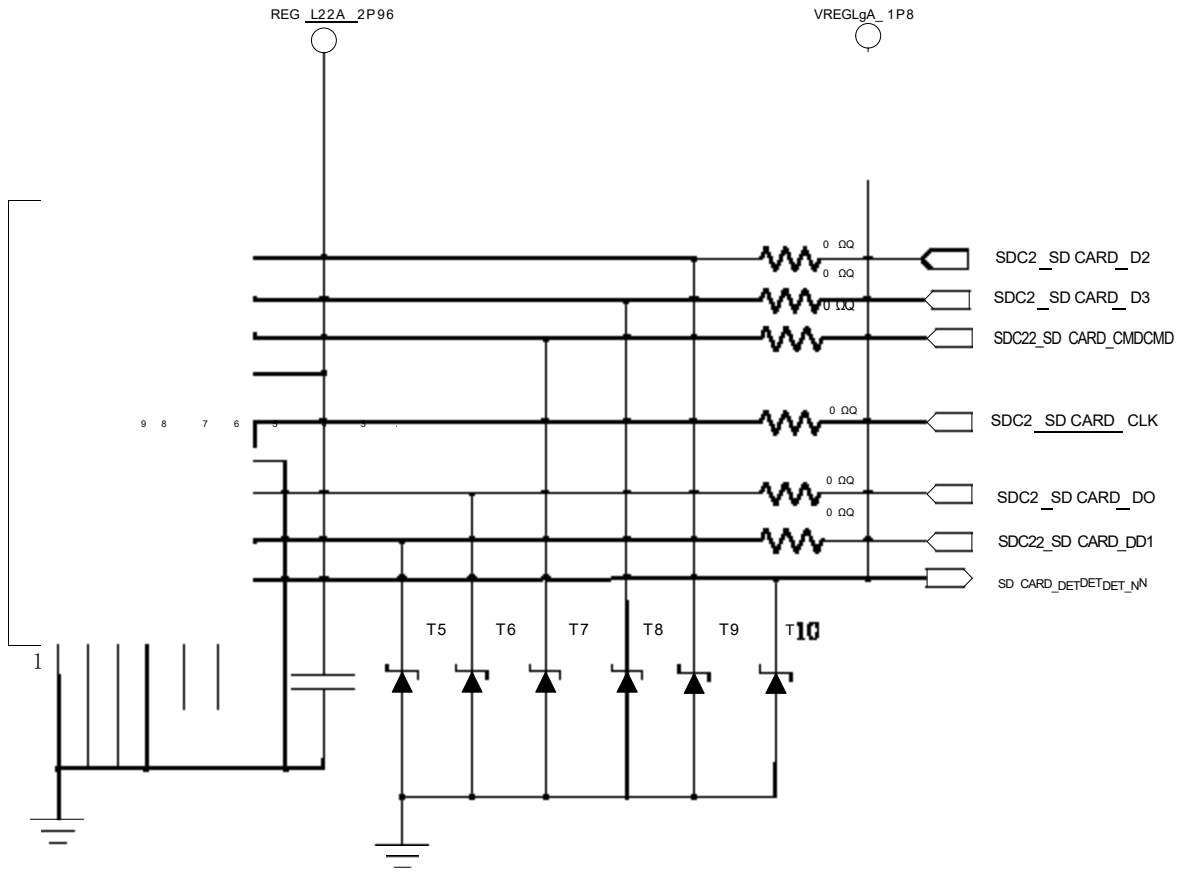


Figure 4.25: SD card interface circuit

4.12. I2C Interface

The SLM927 module supports five I2C interfaces. Pin definitions and default functions are as follows:

Table 4.12: I2C interface pin description

Name	Pins	Default function
TS_I2C_SCL/GPIO7	41	Universal GPIO; TS_I2C clock signal
TS_I2C_SDA/GPIO6*	150/158	General purpose GPIO; TS_I2C data signal
CCI_I2C_SCL0/GPIO23	84	Universal GPIO; Dedicated Camera I2C0 clock signal
CCI_I2C_SDA0/GPIO22	85	Universal GPIO; Dedicated Camera I2C0 data signal
SNS_I2C_SCL/GPIO110	87	Universal GPIO; Dedicated Sensor I2C clock signal
SNS_I2C_SDA/GPIO109*	88	Universal GPIO; Dedicated Sensor I2C data signal
CCI_I2C_SCL1/GPIO30	206	Universal GPIO; Dedicated Camera I2C1 clock signal
CCI_I2C_SDA1/GPIO29	208	Universal GPIO; Dedicated Camera I2C1 data signal
APPS_I2C_SDA/GPIO4*	267	Universal I2C signal, module interior has been pulled up
APPS_I2C_SCL/ GPIO5	268	

Note: Connect 2.2KΩ pull-up resistor to 1.8V when used as I2C bus interface.

4.13. Analog-to-digital Converter (ADC)

SLM927 module by the power management chip to provide 2 ADC input ports ADC/PM6225_GPIO3 (128), ADC/PM6225_GPIO6 (243), its performance parameters are as follows:

Table 4.13: ADC performance parameters

Description	Minimum	Typical value	Maximum value	unit
Input voltage range	0		1.875	V
Analog input bandwidth	-	500	-	kHz
Sampling frequency	-	4.8	-	MHz

4.14. PWM

PWM/PM6225_GPIO8 (44) can be used to make PWM modulation signal of LCD backlight chip, and adjust the backlight brightness by adjusting the duty cycle.

4.15. Antenna Interface

The module provides four antenna interfaces: MAIN antenna, DRX antenna, GPS antenna and WiFi/BT antenna. In order to ensure that the user's product has good wireless performance, the antenna selected by the user should meet the requirements that the input impedance in the working frequency band is 50 ohms, and the standing wave coefficient is less than 2.

4.15.1. MAIN Antenna

The module provides the MAIN antenna interface pin ANT_TRX. The antenna on the user's main board should be connected to the antenna pin of the module using a microstrip line or strip line with a characteristic impedance of 50 ohms.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

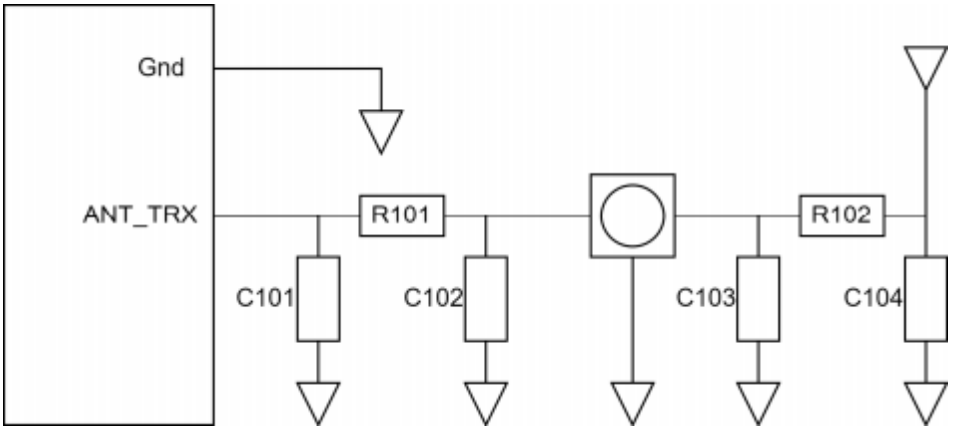


Figure 4.26: TRX antenna interface connection circuit

In the figure, R101, C101, C102 are matching devices, and the specific component values need to be determined after subsequent RF debugging. R102, C103, C104 are antenna matching devices, the specific component values can be determined after the antenna factory debugging the antenna. Among them, R101, R102 default paste 0R, C101, C102, C103, C104 default paste.

If fewer components can be placed between the antenna and the module output, or if the RF test head is not required in the design, the antenna matching circuit can be simplified as shown in the following figure:

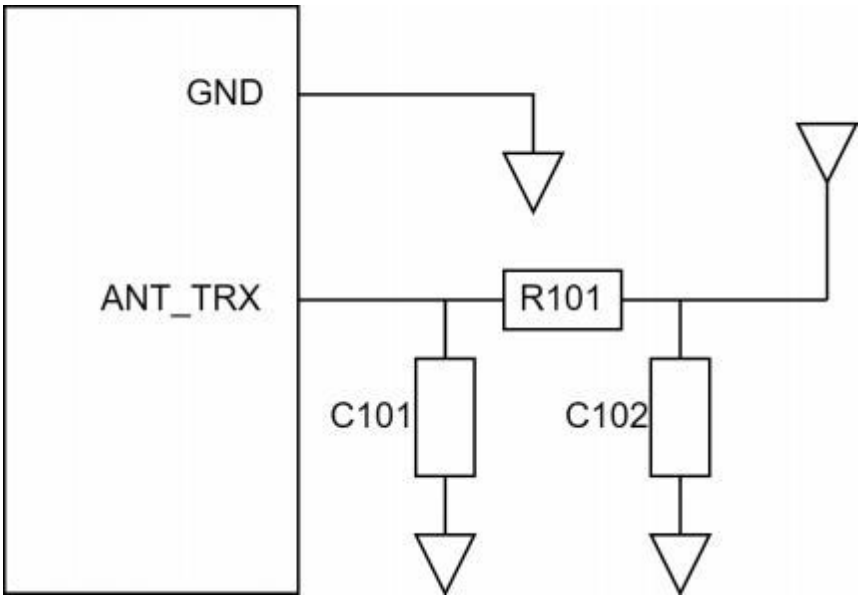


Figure 4.27: Simplified connection circuit for the MAIN antenna interface

In the image above, R101 is pasted 0R by default, C101 and C102 are not pasted by default.

4.15.2. DRX Antenna

DRX antenna interface pin ANT_DRX is provided in the module. The antenna on the user's motherboard should be connected to the antenna pin of the module with a microstrip line or strip line with a characteristic impedance of 50 ohms.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows. In the figure, R101, C101 and C102 are matching devices, and the specific component values need to be determined after subsequent RF debugging. R102, C103, C104 are antenna matching devices, the specific component values can be determined after the antenna factory debugging the antenna. Among them, R101, R102 default paste 0R, C101, C102, C103, C104 default paste.

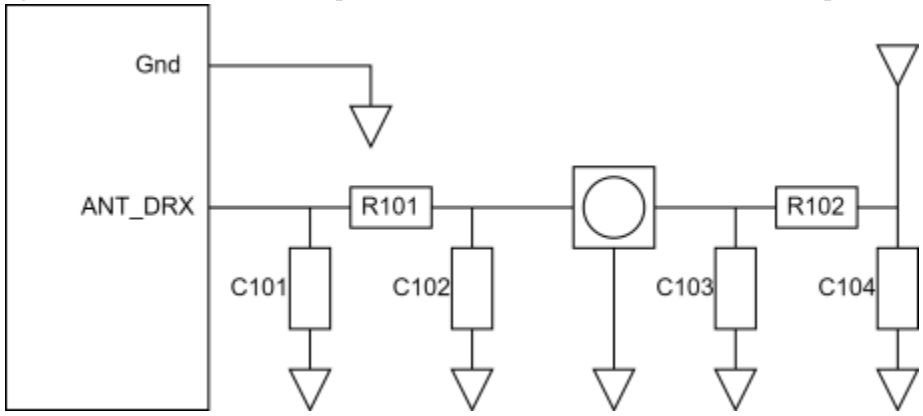


Figure 4.28: DRX antenna interface connection circuit

If there are fewer components that can be placed between the antenna and the module output, or if the RF test head is not required in the design, the antenna matching circuit can be simplified as shown below:

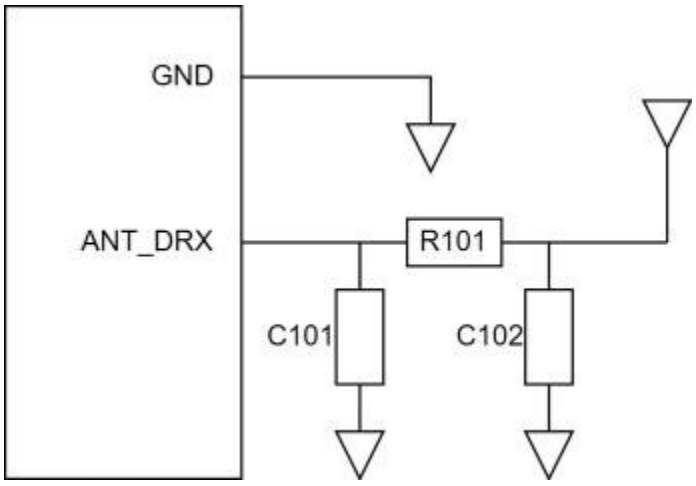


Figure 4.29: DRX antenna interface simplified connection circuit

In the image above, R102 is pasted 0R by default, and C101 and C102 are not.

4.15.3. GPS Antenna

GNSS antenna pin RF_GPS is provided in the module. The antenna on the user's motherboard should be connected to the antenna pin of the module using a microstrip line or strip line with a characteristic impedance of 50 ohms. The LNA is integrated inside the module.

To improve GNSS reception performance, customers can use an external active antenna. The recommended circuit connection is shown in the figure below. In the figure, R101, C101, C102 are matching devices, and the specific component values need to be determined after subsequent RF debugging. R102, L101, L102 are antenna matching devices, and the specific component values can be determined after the antenna is adjusted in the antenna factory. In

addition, the function of C103 to isolate DC must be capacitor, and the function of L103 to isolate RF must be inductor. Among them, R101 and R102 are pasted 0R by default, C101, C102, L101 and L102 are not pasted by default, C103 is 33pF by default, and L103 is 47nF by default.

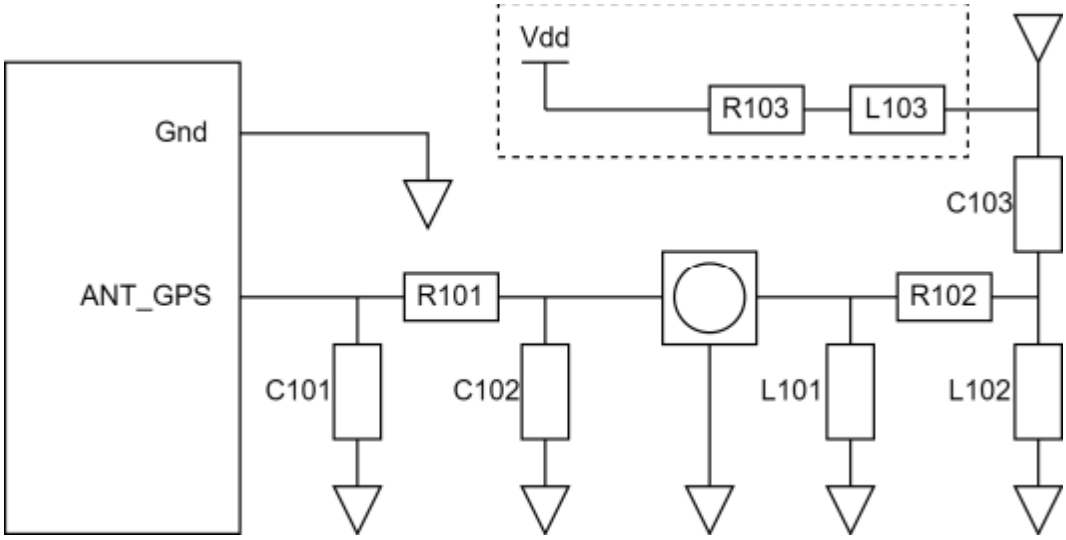


Figure 4.30: Connect an active antenna

4.15.4. WiFi/BT Antenna

The module provides WiFi/BT antenna pin RF_WIFI/BT, and the antenna on the user's motherboard should be connected to the module's antenna pin using a microstrip line or strip line with a characteristic impedance of 50 ohms.

In order to facilitate antenna debugging and certification testing, an RF connector and antenna matching network should be added. The recommended circuit diagram is as follows:

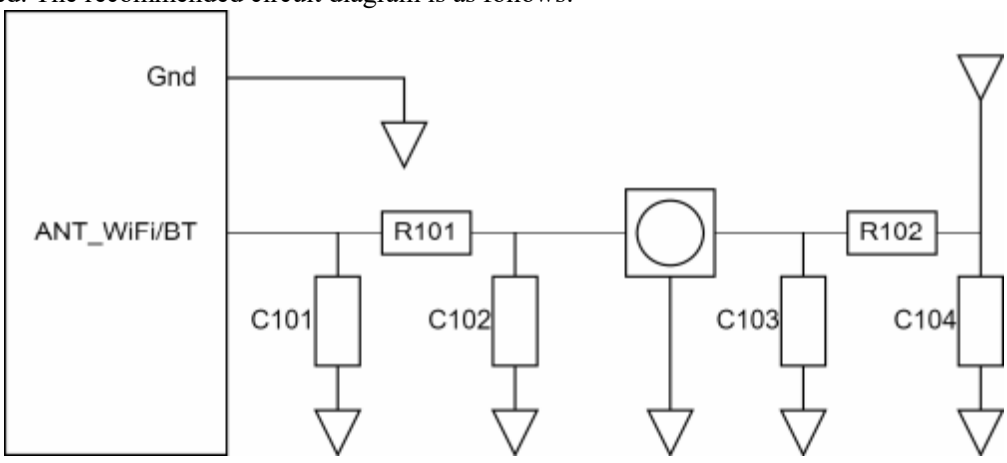


Figure 4.31: WiFI_BT antenna interface connection circuit

R101, C101, C102 are the matching devices, the specific component values need to be determined after the subsequent RF debugging. R102, C103, C104 are antenna matching devices, the specific component values can be determined after the antenna factory commissioning the antenna. Among them, R101, R102 default paste 0R, C101, C102, C103, C104 default paste.

If fewer components can be placed between the antenna and the module output, or if the RF test head is not required in the design, the antenna matching circuit can be simplified as shown in the following figure:

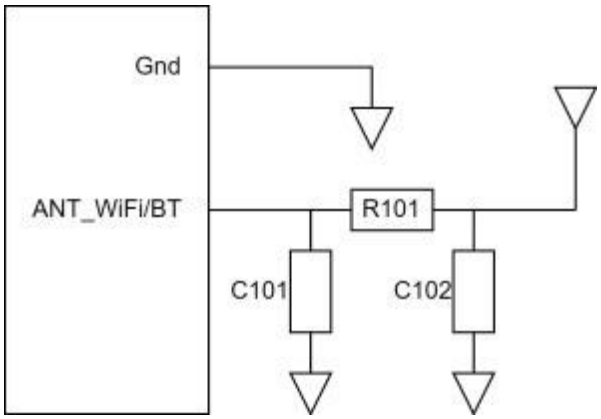


Figure 4.32: WIFI_BT antenna interface simplified connection circuit

In the image above, R301 is pasted 0R by default, C101 and C102 are not.

4.15.5. Antenna PCB Layout

In the antenna design, SLM927 module has four antenna interfaces, namely ANT_TRX, ANT_DRX, ANT_GPS and ANT_WIFI. Attention should be paid to component placement and RF cable routing:

- The RF test head is used to test the conducted RF performance, and should be placed as close as possible to the antenna pin of the module;
- The antenna matching circuit should be placed close to the antenna end;
- The connection between the antenna pin of the module and the antenna matching circuit must be controlled by 50 ohm impedance;
- The device and connection between the antenna pin of the module and the antenna connector must be away from high-speed signal lines and strong interference sources, and avoid crossing or parallel with any signal lines in the adjacent layer.
- The length of the radio frequency line between the antenna pin of the module and the antenna connector should be as short as possible, and the situation of traversing the entire PCB board should be absolutely avoided.
- If the antenna is connected by a coaxial RF line, care should be taken to avoid the coaxial RF line across the SIM card, the power supply circuit and the high-speed digital circuit, so as to minimize the impact between each other.

For user PCBS, the characteristic impedance of all RF signal lines should be controlled at 50 Ω. In general, the impedance of the RF signal line is determined by the dielectric constant of the material, the line width (W), the ground clearance (S), and the height of the reference ground plane (H). PCB characteristic impedance is usually controlled by microstrip line and coplanar waveguide in two ways. In order to reflect the design principles, the following figures show the structural design of the microstrip line and coplanar waveguide when the impedance line is controlled to 50 Ω.

. Complete structure of microstrip line

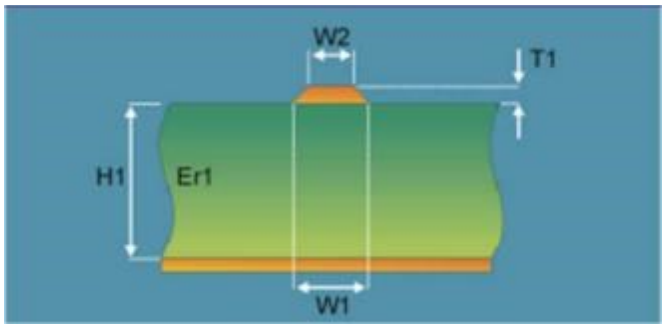


Figure 4.33 Microstrip line structure of two-layer PCB board

. Complete structure of coplanar waveguide

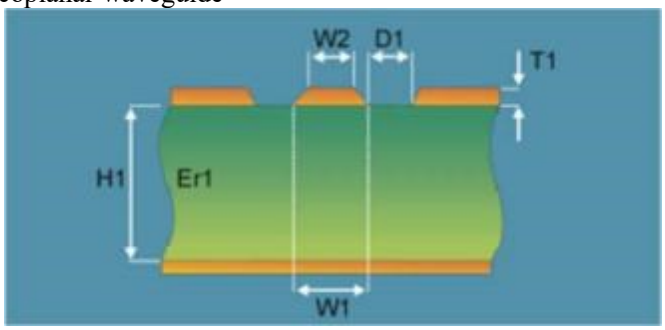


Figure 4.34 Coplanar waveguide structure of two-layer PCB board

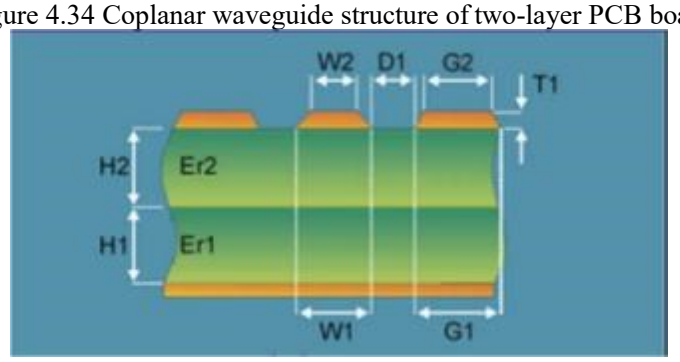


Figure 4.35 Coplanar waveguide structure of multi-layer PCB board (the reference ground is the third layer)

Note:

To ensure communication capability in all bands, attach all antennas.

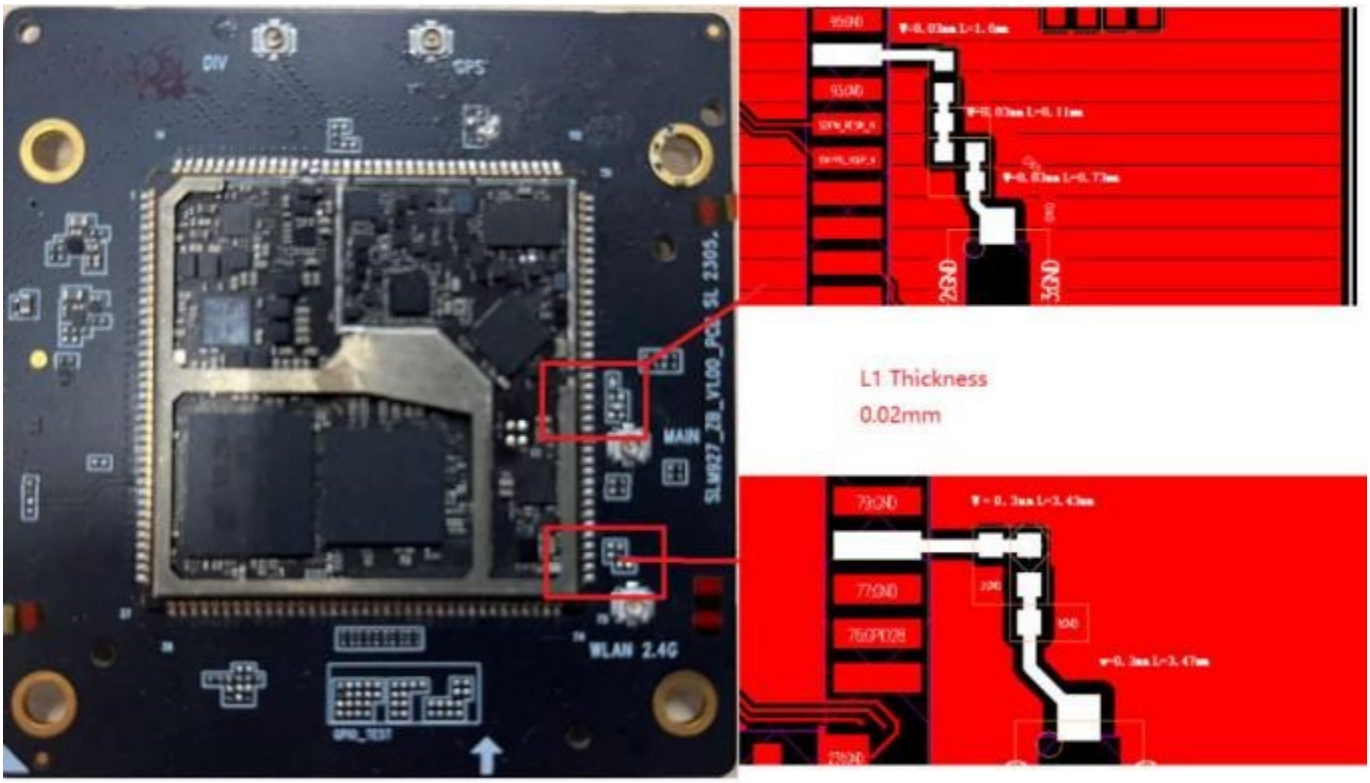
It is recommended that the application side carefully select the RF adapter cable. The RF adapter cable with the lowest possible loss needs to be selected. The following RF conversion cables for RF loss requirements are recommended:

1. FDD-LTE<1.2dB;
2. WIFI/BT < 1.2 dB.

Rf connectors recommended:

Product name		MHF®I LK	MHF®I	MHF®I	MHF®III
Appearance					
		MHF I with mechanical lock	Best Insertion Loss	Most Cable O.D. options	low profile 1.60 mm
Plug part number		-	20767-001R	20278-112R-**	20609-002R
Receptacle part number		20279-001E-** (3 pads) 20441-001E-01 (4 pads)			20369-001E-**
Maximum height (mm)		2.9	3.0	2.5	1.6
Outside dimension of receptacle (mm)		3.0 x 3.0			2.0 x 2.0
Coax O.D. (Center Conductor AWG)	2.00 mm (26)		●		
	1.80 mm (30)	●		●	
	1.37 mm (30)	●		●	
	1.32 mm (32)	●		●	
	1.13 mm (32)	●		●	
	0.95 mm (33)				
	0.81 mm (33)				
	0.81 mm (36)	●		●	●
	0.64 mm (36)				●
	0.48 mm (38)				
Frequency		DC - 9 GHz			DC - 6 GHz
VSWR (L=100mm)	DC - 3GHz	1.3 max.(PLUG) /1.3 max.(RECE)			1.3 max.
	3GHz - 6GHz	1.5 max.(PLUG) /1.4 max.(RECE)			1.5 max.
	6GHz - 9GHz	1.9 max.(PLUG) /1.8 max.(RECE)		1.6 max.(PLUG) 1.8 max.(RECE)	-
	9GHz - 12GHz	-			
	12GHz - 15GHz	-			
Service temp. (Celsius)		-40 degree - 90 degree			
Characteristic impedance		50ohm			
Rated voltage		AC60V			
Contact resistance		20m ohm max.			
Withstand voltage		AC200V/min			
Insulation resistance		500M ohm min./DC100V			

Figure 4.36 RF connector



5. Electrical, Reliability

5.1. Absolute Maximum

The table below shows the absolute maximum values that the module can withstand, exceeding these limits may cause permanent damage to the module.

Table 5.1: Absolute maximum values

Parameters	Minimum value	Typical value	Maximum value	Units
VPH_PWR	0.5	-	6	V
USB_IN_DET	0.3	-	10	V
Peak Current	-	-	3	A

5.2. Operating Temperature

The following table shows the operating temperature range of the module:

Table 5.2: Module operating temperature

Parameters	Minimum value	Typical value	Maximum value	Units
Operating temperature	- 25	-	75	℃
Storage temperature	- 40	-	90	℃

5.3. Operating voltage

Table 5.3: Module operating voltage

Parameters	Minimum value	Typical value	Maximum value	unit
VPH_PWR	3.5	3.8	4.2	V
USB_IN_DET	4	5	6	V

5.4. Digital Interface features

Table 5.4: Digital Interface Characteristics (1.8V)

Parameters	Description	Minimum	Typical value	Maximum value	Units
V_{IH}	Enter the high level voltage	1.17	1.8	2.1	V
V_{IL}	Input the low-level voltage	0.3	0	0.63	V
V_{OH}	Output high level voltage	1.35	-	1.8	V
V_{OL}	Output low voltage	0	-	0.45	V

5.5. Characteristics Of SIM_VDD

Table 5.5: SIM_VDD characteristics

Parameters	Description	Minimum	Typical value	Maximum value	Units
V_O	Output voltage	1.65	1.8	1.95	V
		-	2.95	-	
I_O	Output current	-	-	100	mA

5.6. Features Of KYPD_PWR_N

Table 6.6: KYPD_PWR_N characteristics

Parameters	Description	Minimum	Typical value	Maximum value	Units
KYPD_PWR_N	High	1.4	-	-	V
	Low level	-	-	0.6	V
	Effective time	3000			ms

5.7. Features Of VCOIN

Table 5.7: VCOIN Characteristics

Parameters	Description	Minimum	Typical value	Maximum value	Units
VCOIN-IN	VCOIN input voltage	2.5	3.0	3.1	V
VCOIN-OUT	VCOIN output voltage	-	3.0	-	V

5.8. Electrostatic Protection

The module is not specifically protected against electrostatic discharge. Therefore, users must pay attention to electrostatic protection when producing, assembling and operating modules.

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5.9. Module working frequency band

The following table lists the operating frequency band of the module, which conforms to the 3GPP TS 05.05 technical specification.
Table 5.9 : Module operating frequency bands

5.10. Key RF Performance Of GNSS

The following table lists the main RF properties of GNSS conduction.

Table 6.14: Main RF performance parameters under GNSS conduction

GNSS operating band :1575.42MHZ				
GNSS load/noise ratio CN0:39dB /Hz				
GNSS sensitivity:	Capture (cold start)	Capture (hot start)	Track	
	- 148.	- 156.	- 160.	dBm
GNSS startup time	Hot Start	Warm Start	Cold start	
	TBD	TBD	TBD	

5.11. Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to LANDI that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:

Contains FCC ID:2AG6N-SLM927AM4MG The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna Manufacturer	Antenna Type	Input Impedance (Ohm)	Frequency Range	Antenna Gain
Jesoncom	FPC Antenna	50	2402-2480MHz	0.84dBi(BT)
Jesoncom	FPC Antenna	50	2402-2480MHz	0.84dBi(BLE)
Jesoncom	FPC Antenna	50	2412-2462MHz	0.84dBi(2.4G WIFI)
Jesoncom	FPC Antenna	50	5150-5250MHz, 5250-5350MHz, 5470-5725MHz, 5725-5850MHz	0.95dBi(5G WIFI)
Jesoncom	FPC Antenna	50	617~2690MHz	5.14dBi(LTE)

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manualshall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following twoconditions:

(1) This device may not cause harmful interference.

(2) this device must accept any interference received, including interference that may cause undesired operation. This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, 15.247 and 15.407 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitterrules) listed on the grant, and that the host product manufacturer is responsible for compliance toany other FCC rules that apply to the host not covered by the modular transmitter grant ofcertification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following

conditions:

(For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This equipment should be installed and operated with minimum distance 20 cm between the radiator &your body.

6. Production

6.1. Top and Bottom Views of the Module

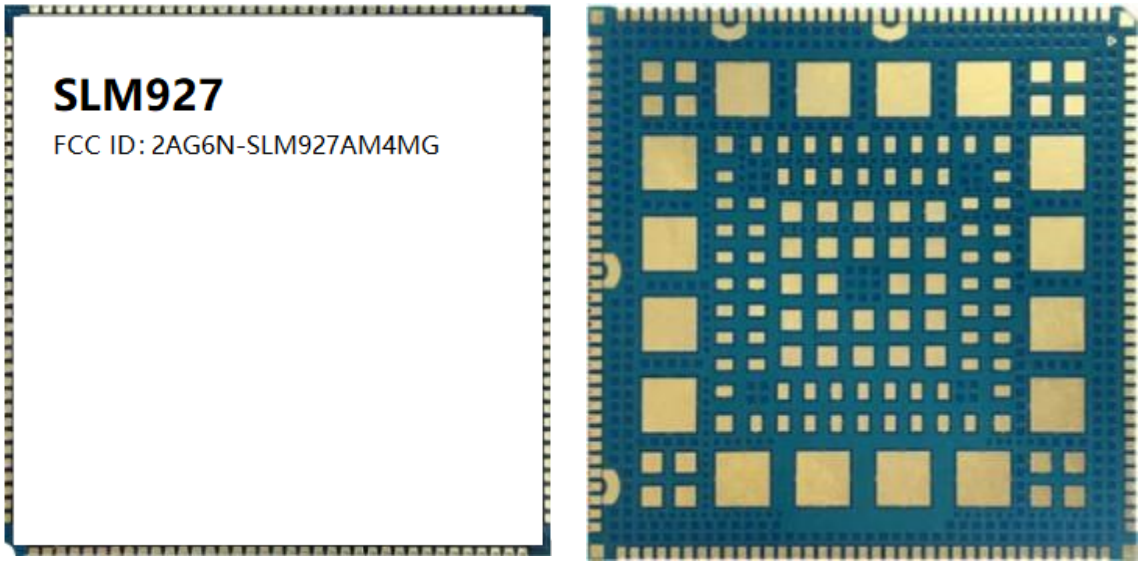
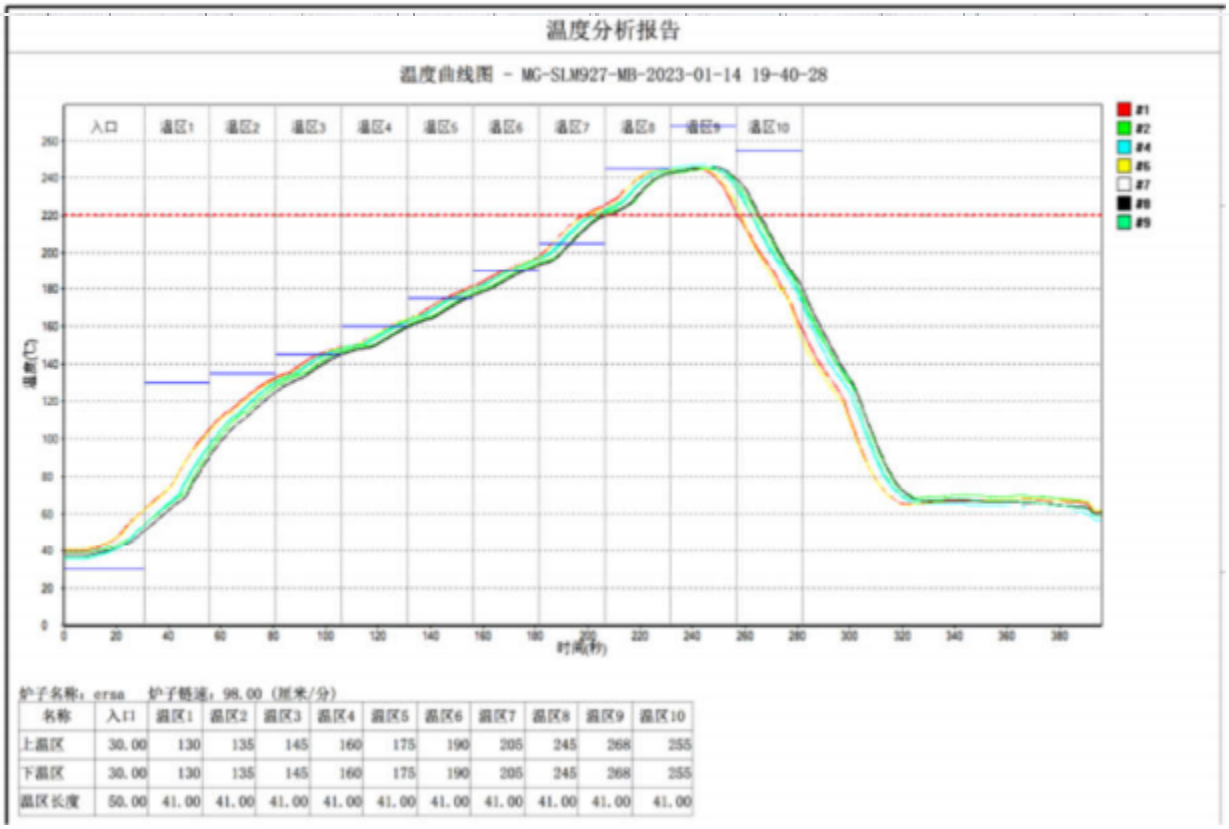


Figure 6.1: Top view and bottom view of the module

6.2. Recommended Welding Furnace Temperature Curve



名称	入口	温区1	温区2	温区3	温区4	温区5	温区6	温区7	温区8	温区9	温区10
上温区	30.00	130	135	145	160	175	190	205	245	268	255
下温区	30.00	130	135	145	160	175	190	205	245	268	255
温区长度	50.00	41.00	41.00	41.00	41.00	41.00	41.00	41.00	41.00	41.00	41.00

Figure 6.2: Recommended soldering furnace temperature curve for modules

6.3. Moisture Sensitive Characteristics (MSL)

The SLM927 module meets humidity sensitivity level 3. Dry packaging performs J-STD-020C specification according to IPC/JEDEC standard under ambient conditions of <30 degrees and relative humidity <60%. At ambient conditions of <40 degrees and <90% relative humidity, the shelf life is at least 6 months when unopened. After unpacking, Table 22 lists the shelf life times of the modules corresponding to different humidity sensitivity levels.

Table 6.1: Classification of humidity sensitivity levels

Levels	Factory environment ≦+30℃/60%RH
1	Indefinite warranty in the environment ≦+30℃/85% RH conditions
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Force bake before using. After baking, the module must be mounted within the time limit specified on the label.

After unpacking, it takes 168 hours for SMT to be applied under ambient conditions of <30 degrees and relative humidity <60%. If the above conditions are not met, bake. Note: Oxidation risk: Baking SMD packages may cause metal oxidation and, if excessive, can cause solderability problems during board assembly. Baking SMD packages for temperature and time, therefore limits solderability considerations. The accumulation of baking time at temperatures greater than 90°C and up to 125°C should not exceed 96 hours.

6.4. Baking Demand

Due to the humidity sensitive nature of the module, the SLM927 should be fully baked prior to reflow soldering, otherwise the module may cause permanent damage during reflow soldering. The SLM927 should be baked for 192 hours in a low temperature container with a temperature of 40°C +5°C /-0°C and a relative humidity of less than 5%, or for 72 hours in a high temperature container with the module at 80°C±5°C. The user should note that the tray is not resistant to high temperatures and the user should take the module out of the tray for baking, otherwise the tray maybe damaged by high temperatures.

Table 6.2: Baking requirements:

Baking temperature	humidness	Baking time
40°C±5°C	< 5%	192 hours
120°C±5°C	< 5%	4 hours

7. Appendix

7.1. Related Documentation

Table 9.1: Relevant documentation

Serial number	Document name	Comments
[1]	GSM 07.07:	Digital cellular telecommunications (Phase 2+); AT command set for GSM Mobile Equipment (ME)
[2]	GSM 07.10:	Support GSM 07.10 multiplexing protocol
[3]	GSM 07.05:	Digital cellular telecommunications(Phase 2+); Use of Data Terminal Equipment–Data Circuit terminating Equipment(DTE–DCE) interface for Short Message service(SMS)and Cell Broadcast Service(CBS)
[4]	GSM 11.14:	Digital cellular telecommunications system (Phase 2+); Specification of the SIM Application Toolkit for the Subscriber Identity Module–Mobile Equipment (SIM–ME) interface
[5]	GSM 11.11:	Digital cellular telecommunications system (Phase 2+); Specification of the Subscriber Identity Module – Mobile Equipment (SIM–ME) interface
[6]	GSM 03.38:	Digital cellular telecommunications system (Phase 2+); Alphabets and language-specific information
[7]	GSM 11.10	Digital cellular telecommunications system (Phase 2); Mobile Station (MS) conformance specification; Part 1: Conformance specification
[8]	AN_Serial Port	AN_Serial Port

7.2. Terminology And Explanation

Table 9.2: Terminology and interpretation

Terms	Explanations
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DTE	Data Terminal Equipment (typically computer, terminal, printer)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission

EFR	Enhanced Full Rate
EGSM	Enhanced GSM
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
FR	Full Rate
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
IMEI	International Mobile Equipment Identity
Li-ion	Lithium-Ion
MO	Mobile Originated
MS	Mobile Station (GSM engine), also referred to as TE
MT	Mobile Terminated
PAP	Password Authentication Protocol
PBCCH	Packet Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PPP	Point-to-point protocol
RF	Radio Frequency
RMS	Root Mean Square (value)
RX	Receive Direction
SIM	Subscriber Identification Module
SMS	Short Message Service
TDD	Time Division Distortion
TE	Terminal Equipment, also referred to as DTE
TX	Transmit Direction
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
FD	SIM fix dialing phonebook
LD	SIM last dialing phonebook (list of numbers most recently dialed)
MC	Mobile Equipment list of unanswered MT calls (missed calls)
ON	SIM (or ME) own numbers (MSISDNs) list
RC	Mobile Equipment list of received calls
SM	SIM phonebook

NC	Not connect