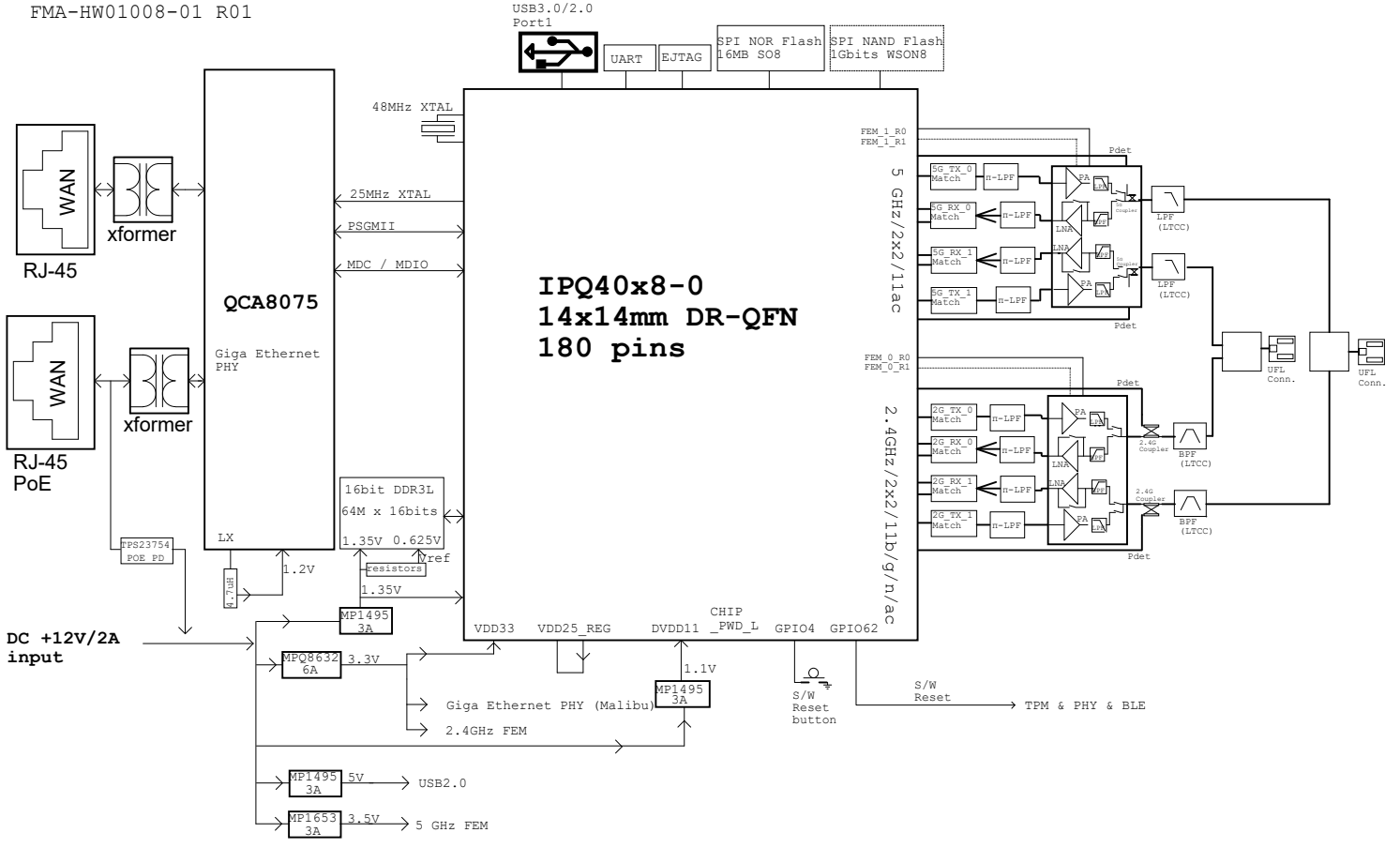
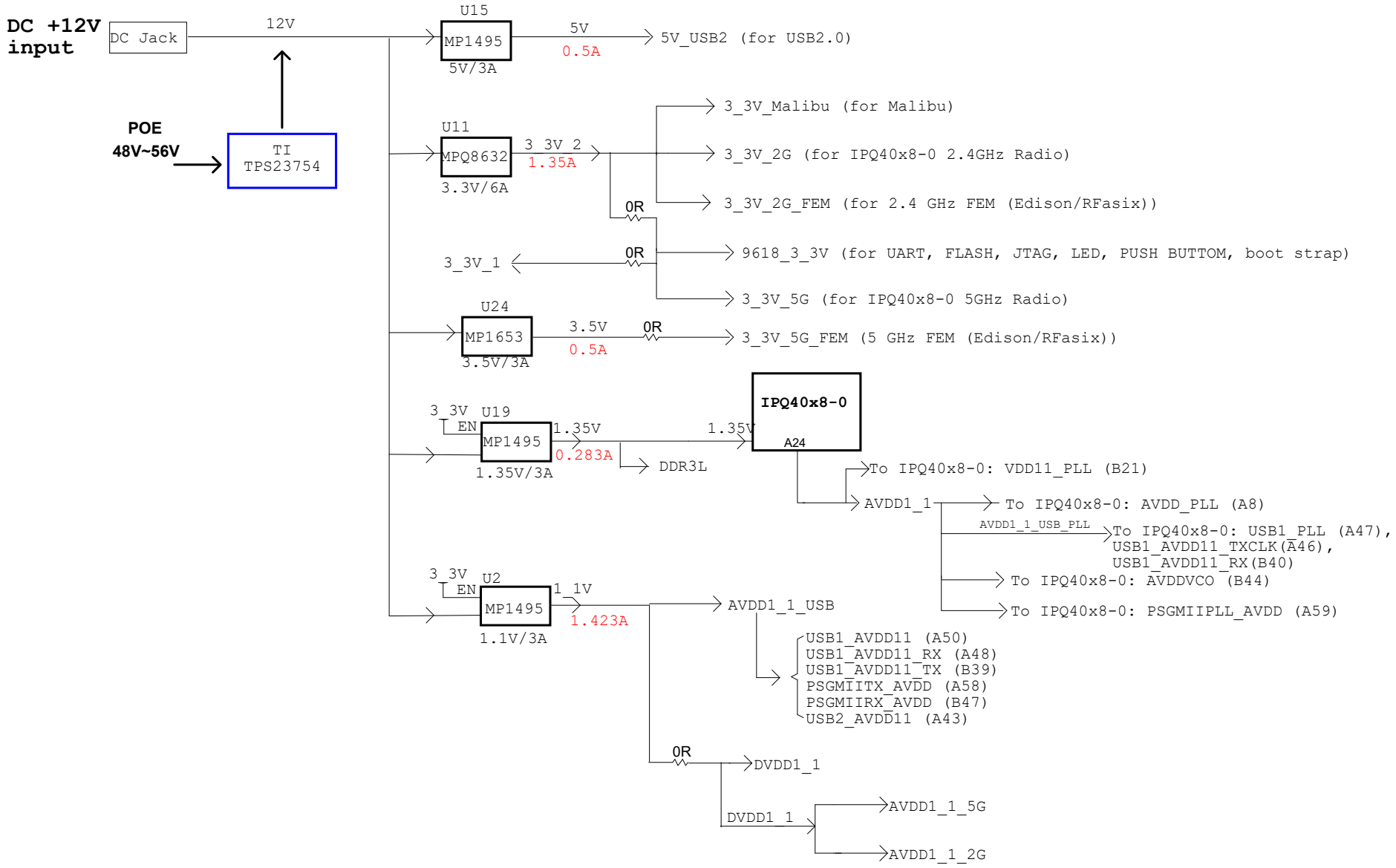
FMA-HW01008-01 R01



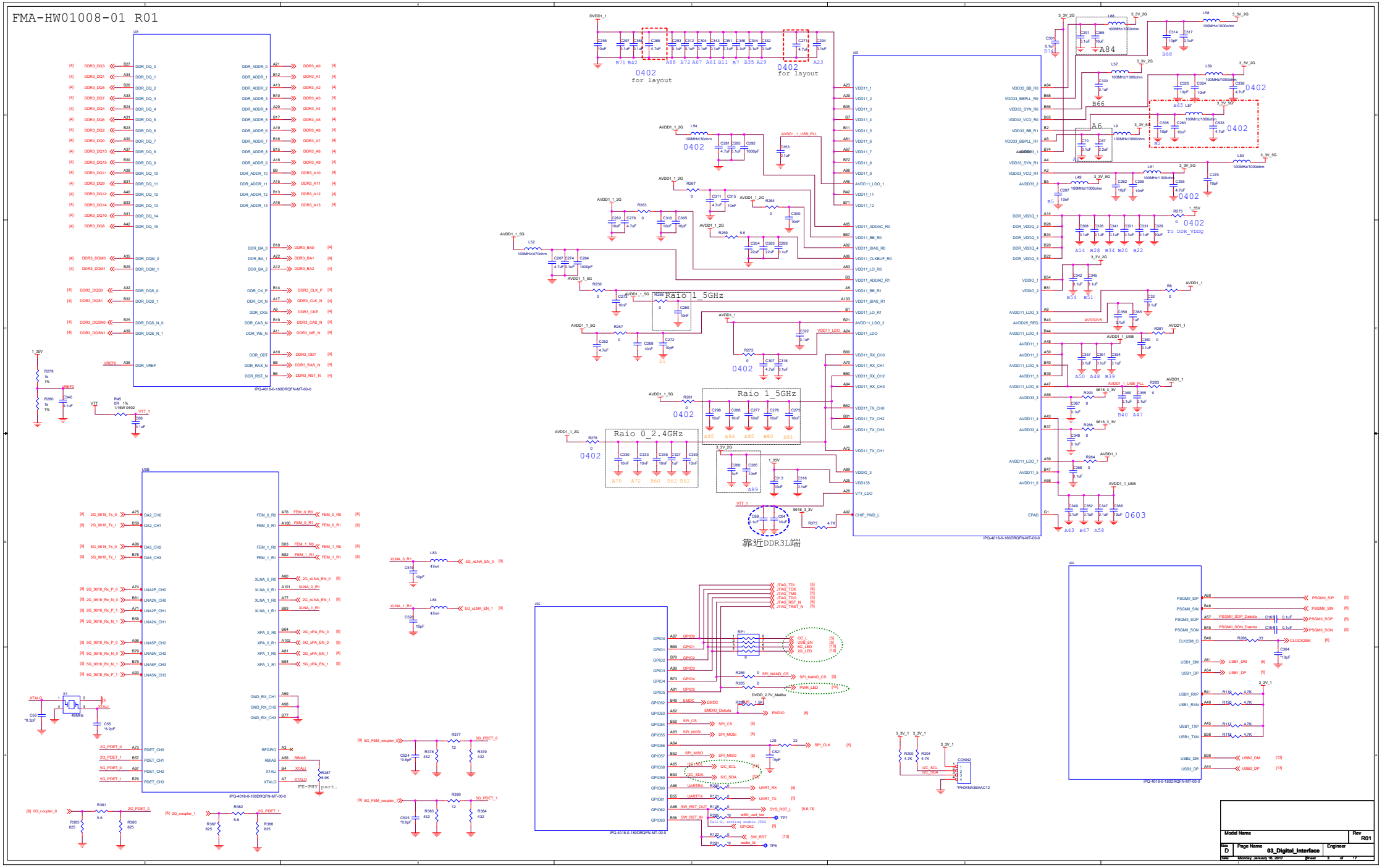
Model Name		Rev R01
Size D	Page Name 01_BLOCK DIAGRAM	Engineer
Date Monday, January 16, 2017	Sheet 1 of 17	

FMA-HW01008-01 R01

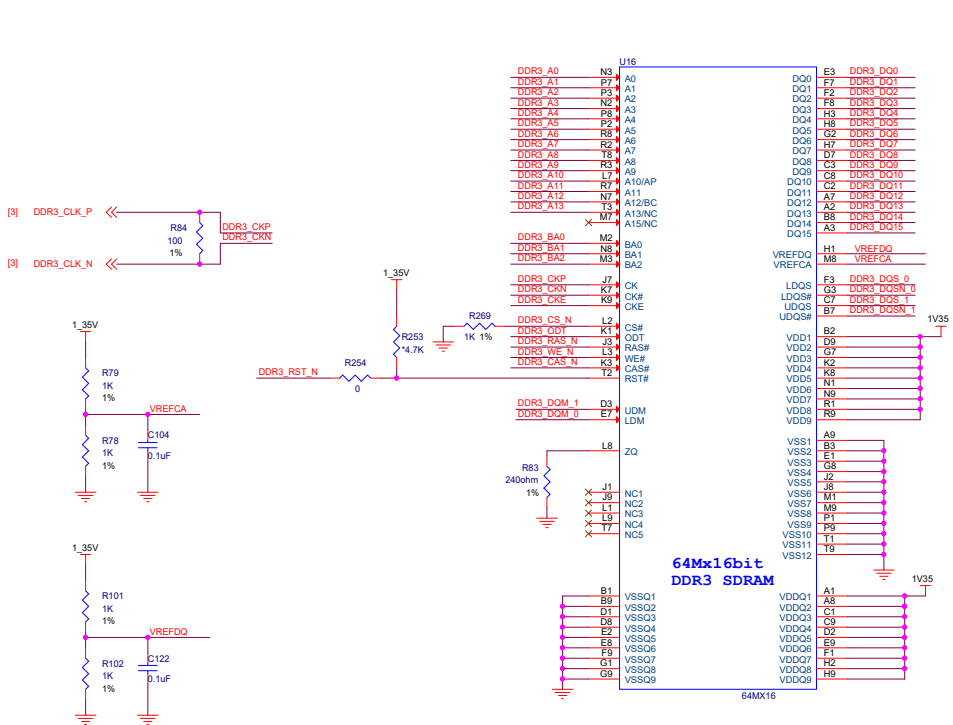


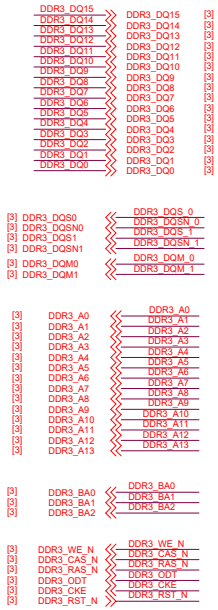
Model Name		Rev R01
Size C	Page Name 02_Power Tree	Engineer
Date: Monday, January 16, 2017	Sheet 2 of 17	

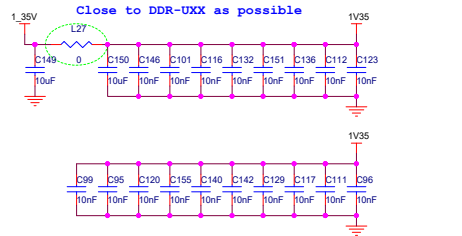
FMA-HW01008-01 R01

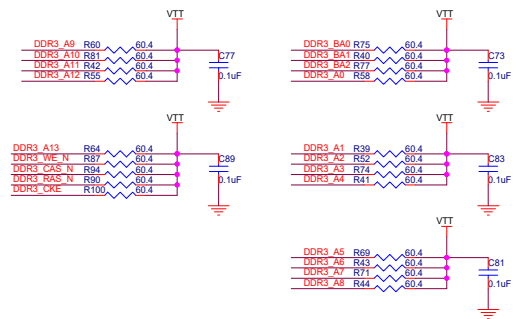


FMA-HW01008-01 R01









Model Name		Rev R01
Size C	Page Name 04_DDR3	Engineer
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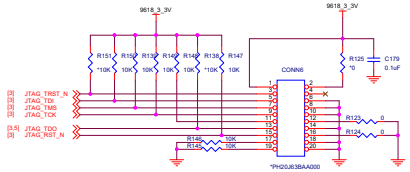
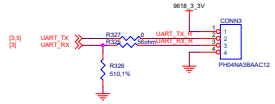
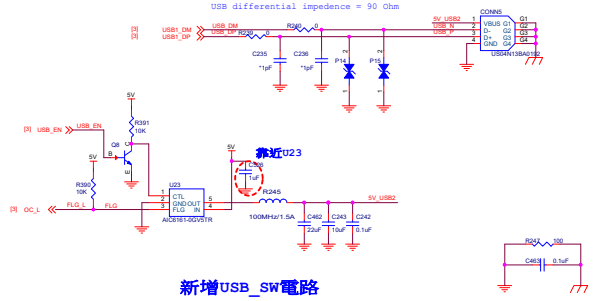


20-PIN ARM JTAG Connector

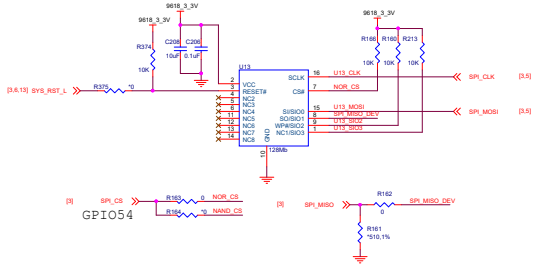


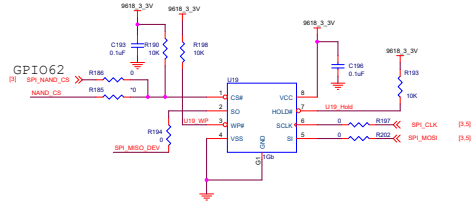
UART



新增USB_SW電路

SPI NOR 16MB

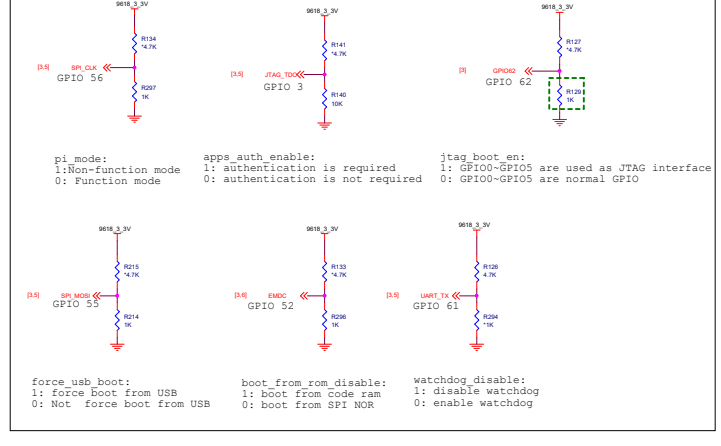




SPI NAND Flash_1Gbits

	控制訊號	上件電阻
SPI NOR (16M or 32M)	GPIO54	R163
SPI NAND (1Gb)	GPIO4	R164
SPI NOR (16M) + SPI NAND (1Gb)	NOR: GPIO54 NAND: GPIO4	R163 and R186

Boot Strap



Model Name		Rev R01
Size D	Page Name 05_EJTAG_USB_UART_NOR_CSTRAP	Engineer
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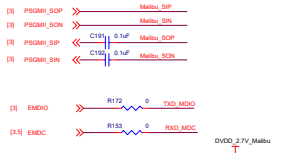
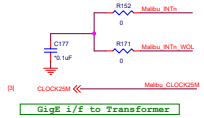
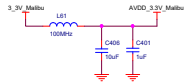
PSGMII i/f to QCA9618

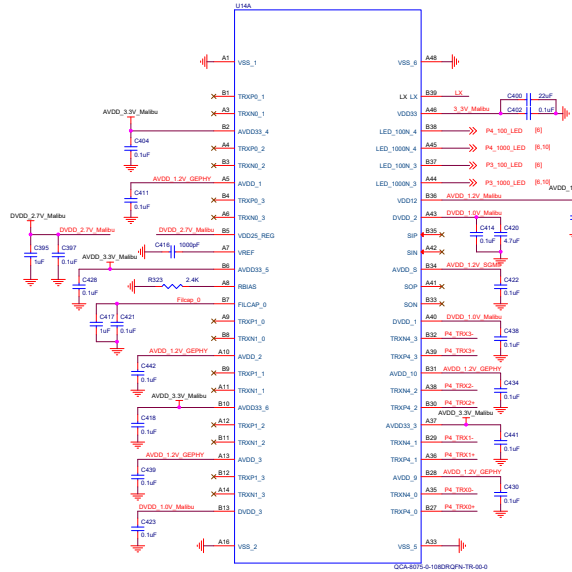


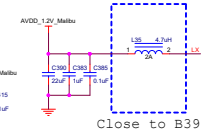
RC delay when R134& C174 No_Load.

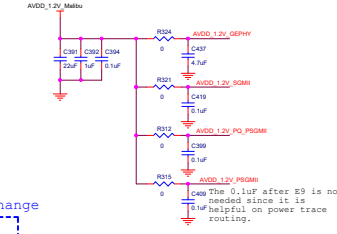


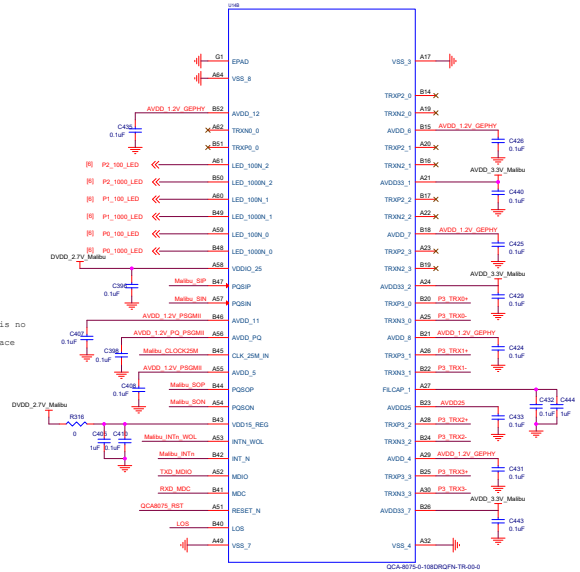
GigE i/f to Transformer







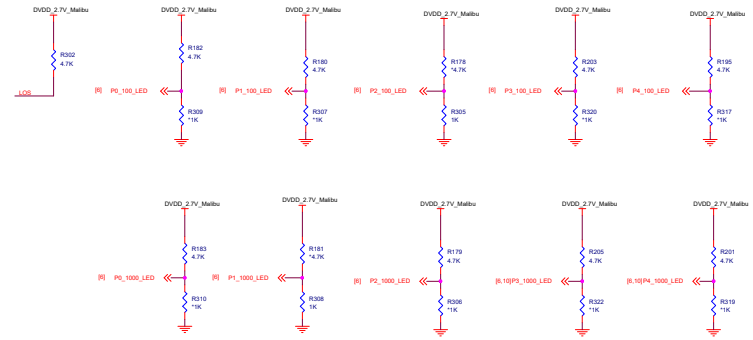




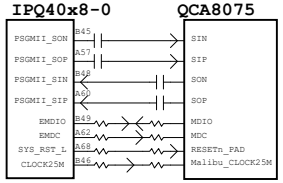
Power strapping

PAD	Pull UP/DOWN(default)	internal signal
DPAD_LED_LINK100n_0	UP	mode1_pos
DPAD_LED_LINK1000n_0	UP	mode2_pos
DPAD_LED_LINK100n_1	UP	mode3_pos
DPAD_LED_LINK1000n_1	down	phyaddress_reg[3]
DPAD_LED_LINK100n_2	down	phyaddress_reg[4]
DPAD_LED_LINK1000n_2	UP	control_dac_pos[0]
DPAD_LED_LINK100n_3	UP	control_dac_pos[1]
DPAD_LED_LINK1000n_3	UP	control_dac_pos[2]
DPAD_LED_LINK100n_4	UP	az_sel_pos
DPAD_LED_LINK1000n_4	UP	idac_adj[2]

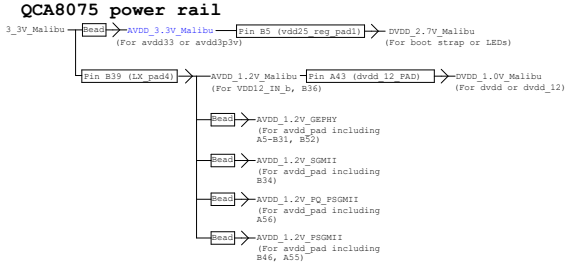
Boot Strap



IPQ40x8-0 — QCA8075



QCA8075 power rail



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Size D	Page Name 06_Malibu_Giga_PHY		Engineer
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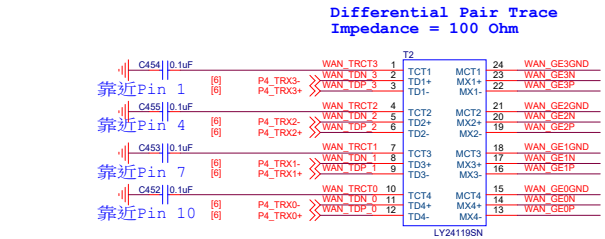

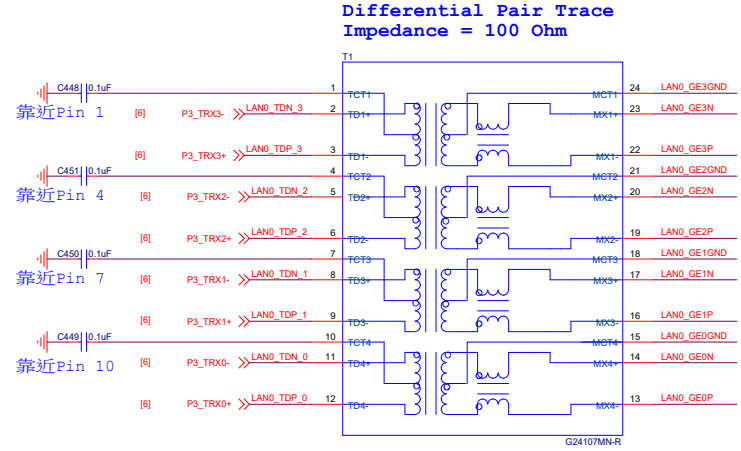

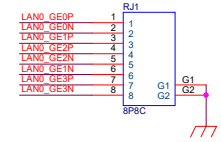

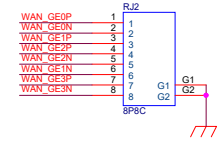

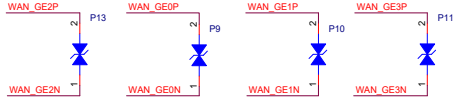

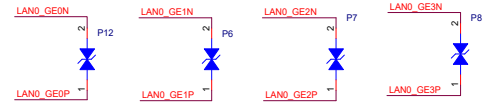

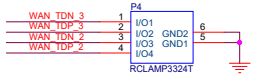

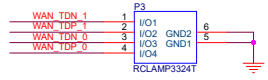

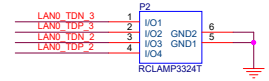

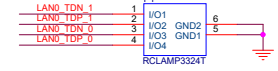

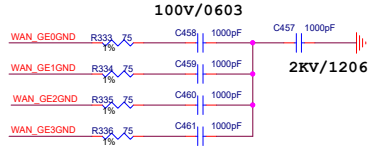

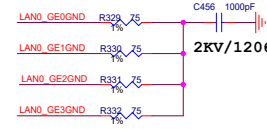

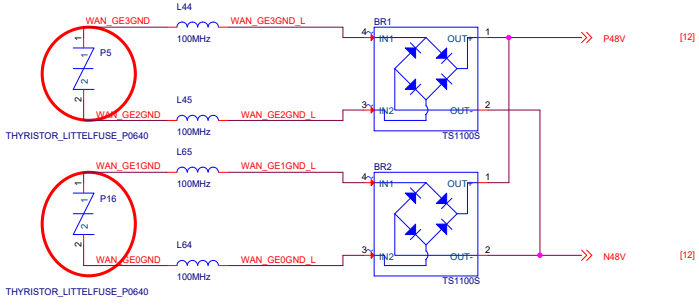

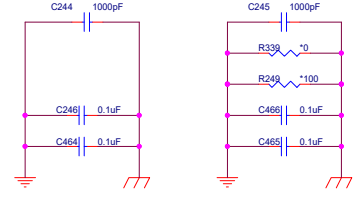

Model Name		Rev R01
Size C	Page Name 07_Malibu_Ethernet_Magnetics	Engineer
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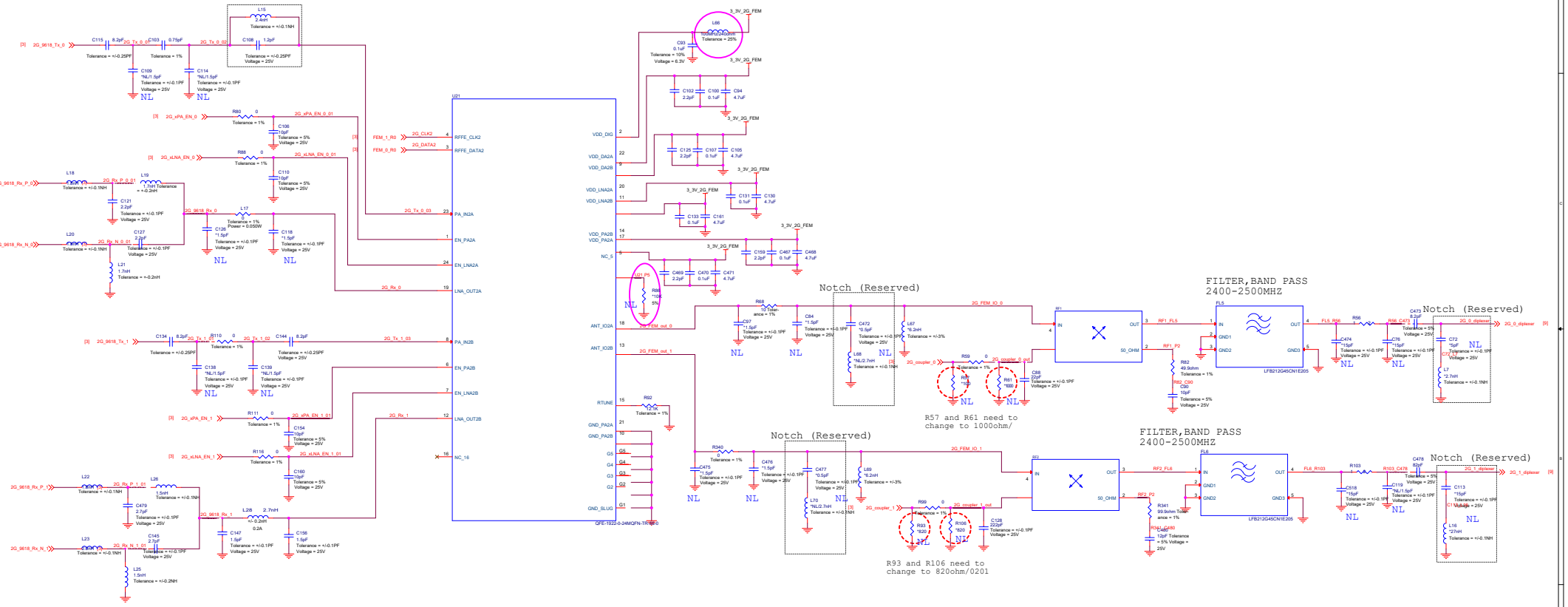

Model Name			Rev R01
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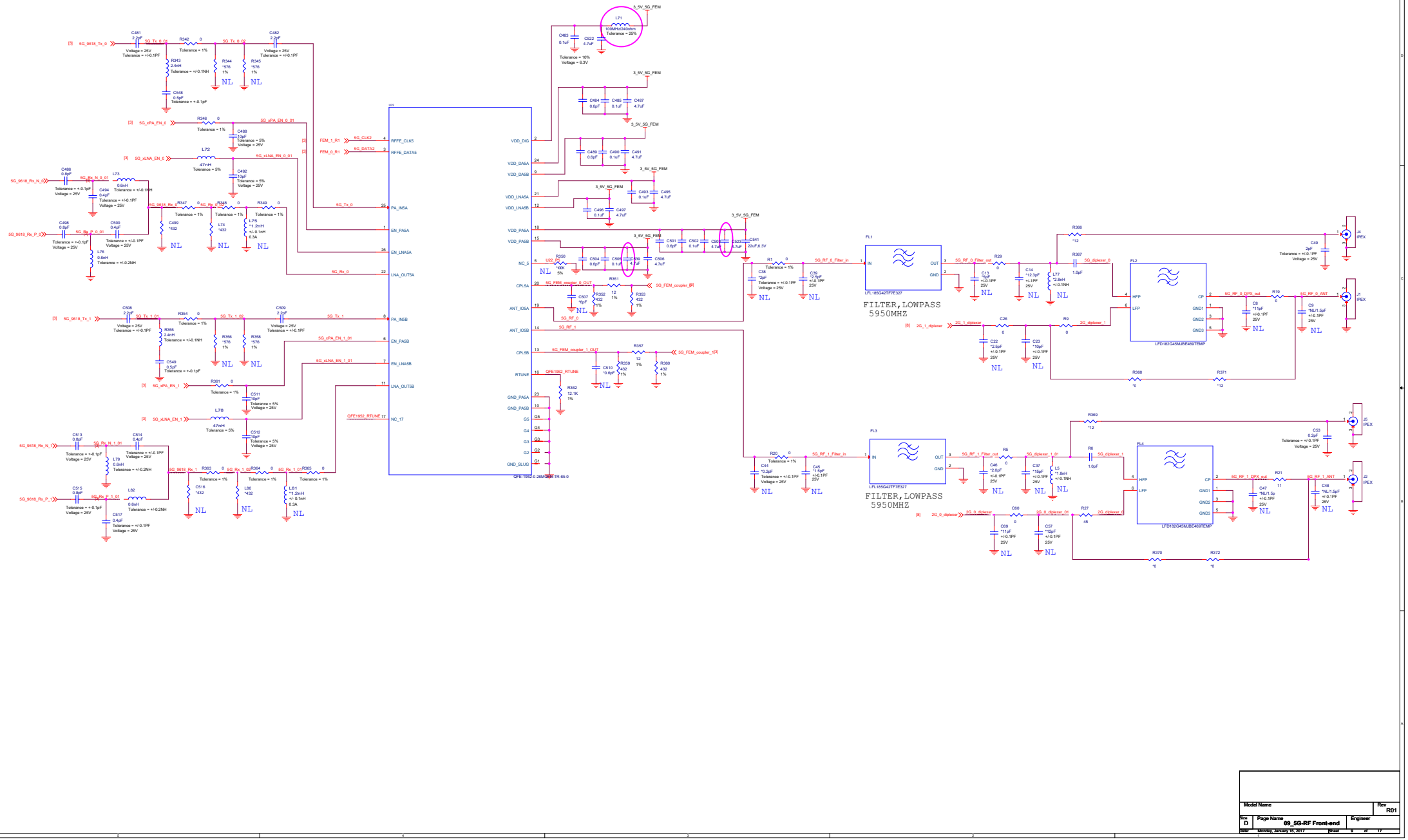
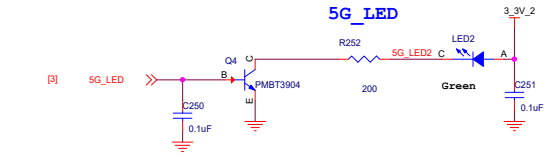
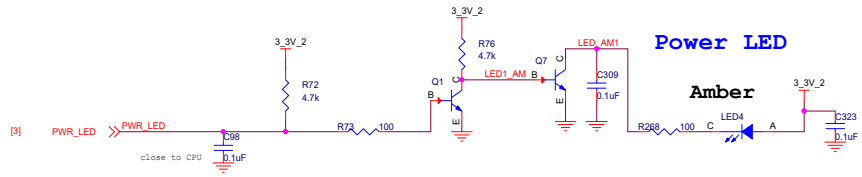
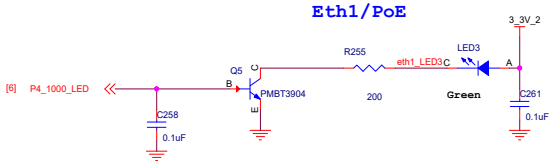
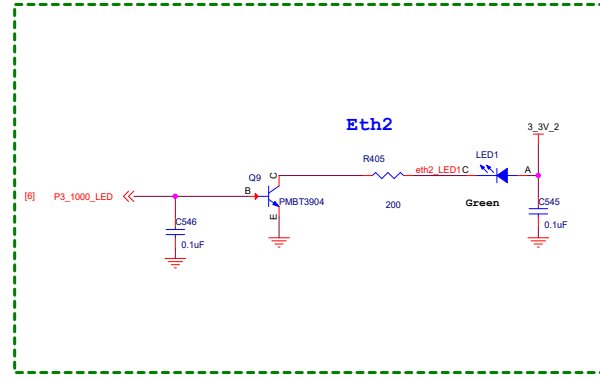


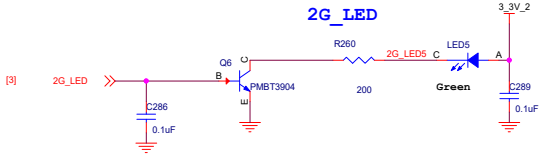
FMA-HW01008-01 R01

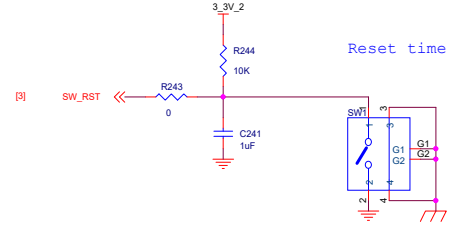






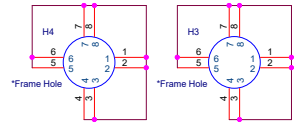




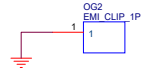


Reset time must more than 10ms to CHIP_PWD_L

S/W RESET
Manufactory default reset



MTH_197C106D_8DP



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Size C	Page Name 10_MISC_I2S_LED	Engineer
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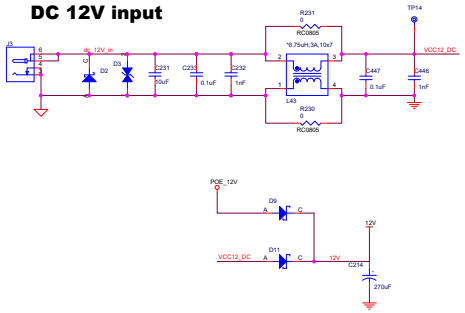
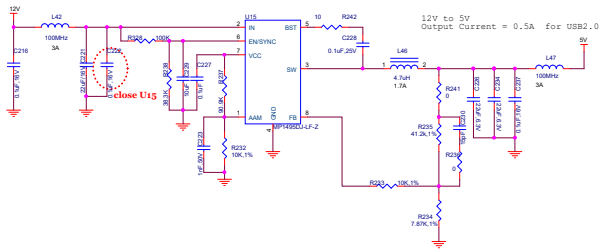
DC 12V input



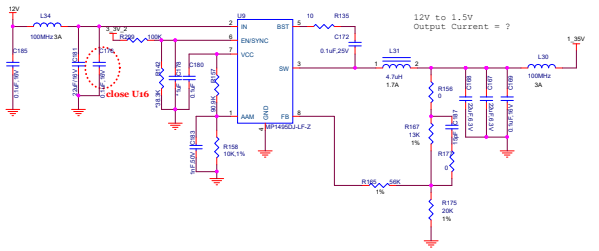
12V to 5V for USB3.0 & 2.0

VCC5.0 = 0.807*(1+41.2k/7.86k)=5.037V

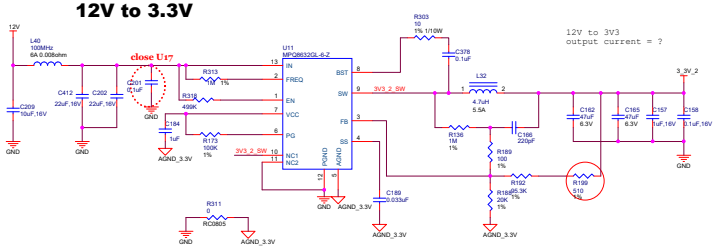


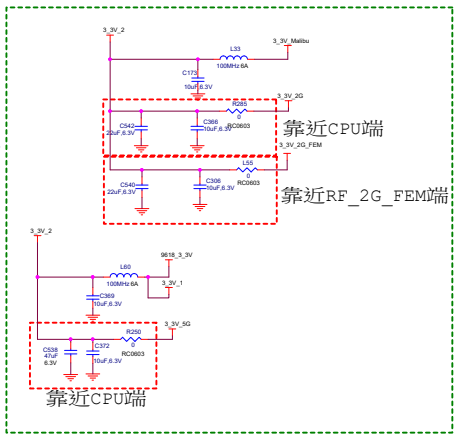
12V to 1.35V for DDRIIIL

VCC 1.35V = 0.807*[1+(13K+0.51K)/20k]=1.3517V



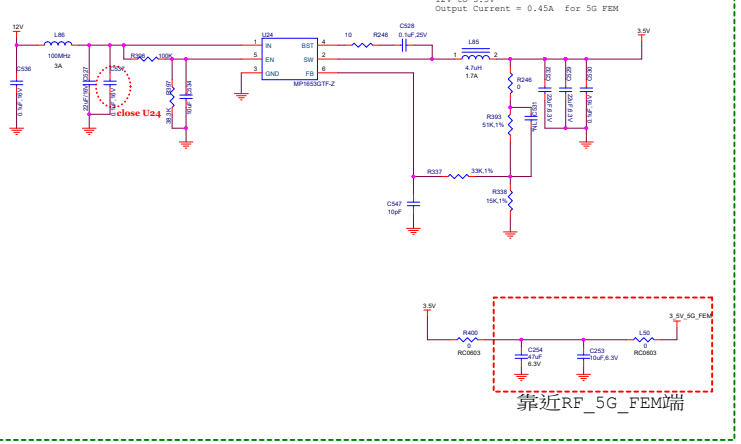
12V to 3.3V





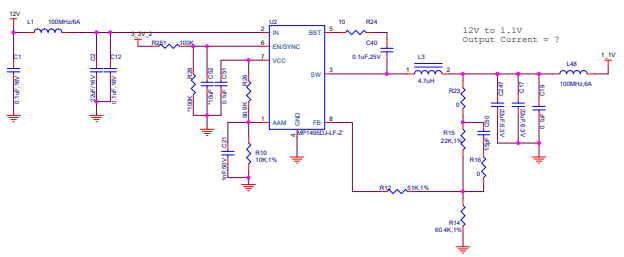
12V to 3.5V for 5G FEM

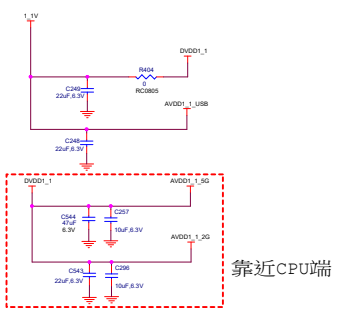
VCC5.0 = 0.8*(1+51k/15k)=3.52V



12V to 1.1V

VCC1.1 = 0.807*[1+22k/60.4k] = 1.1V





Model Name		Rev R01
Size D	Page Name 11_Power Regulator	Engineer
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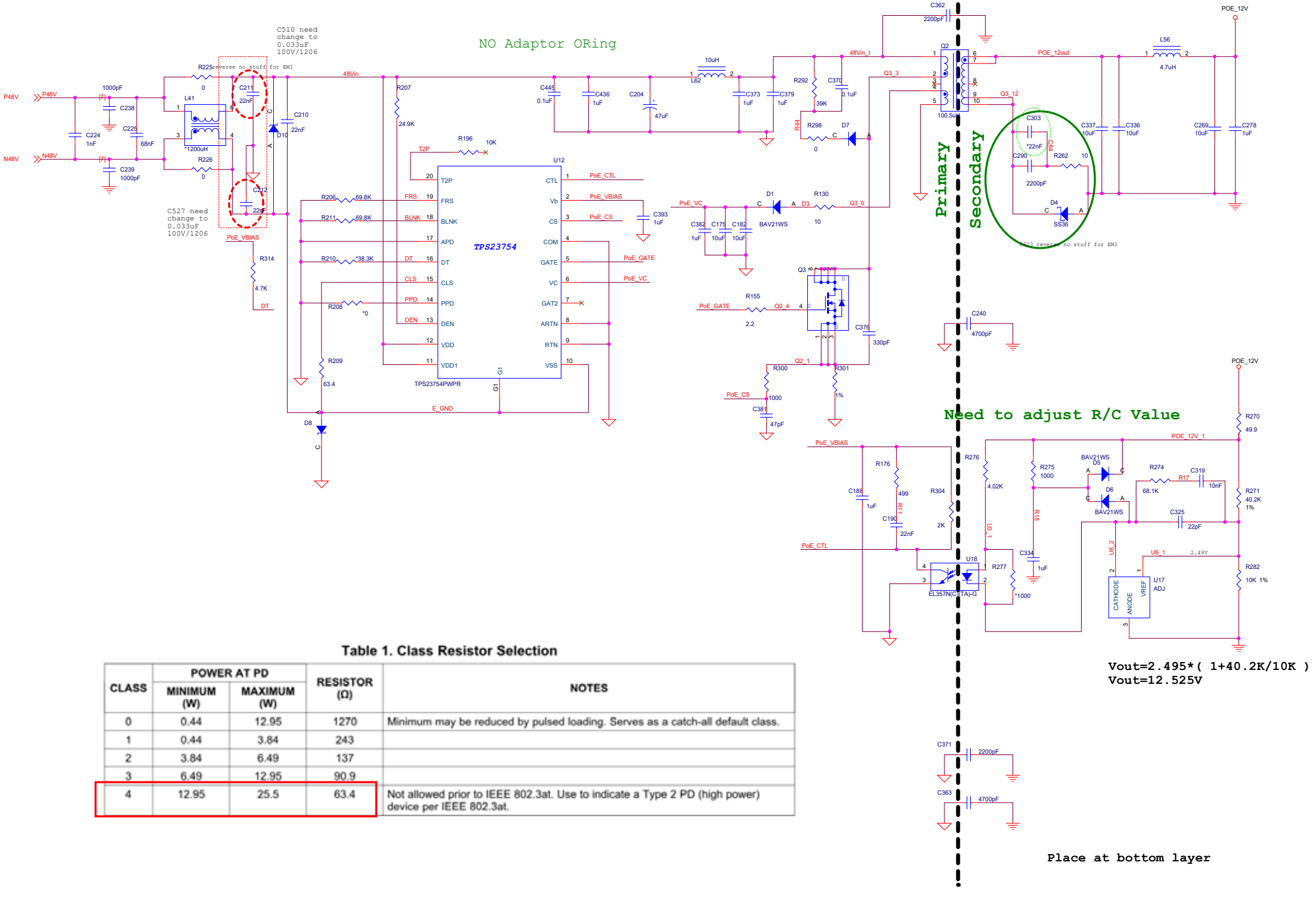

Table 1. Class Resistor Selection

CLASS	POWER AT PD		RESISTOR (Ω)	NOTES
	MINIMUM (W)	MAXIMUM (W)		
0	0.44	12.95	1270	Minimum may be reduced by pulsed loading. Serves as a catch-all default class.
1	0.44	3.84	243	
2	3.84	6.49	137	
3	6.49	12.95	90.9	
4	12.95	25.5	63.4	Not allowed prior to IEEE 802.3at. Use to indicate a Type 2 PD (high power) device per IEEE 802.3at.

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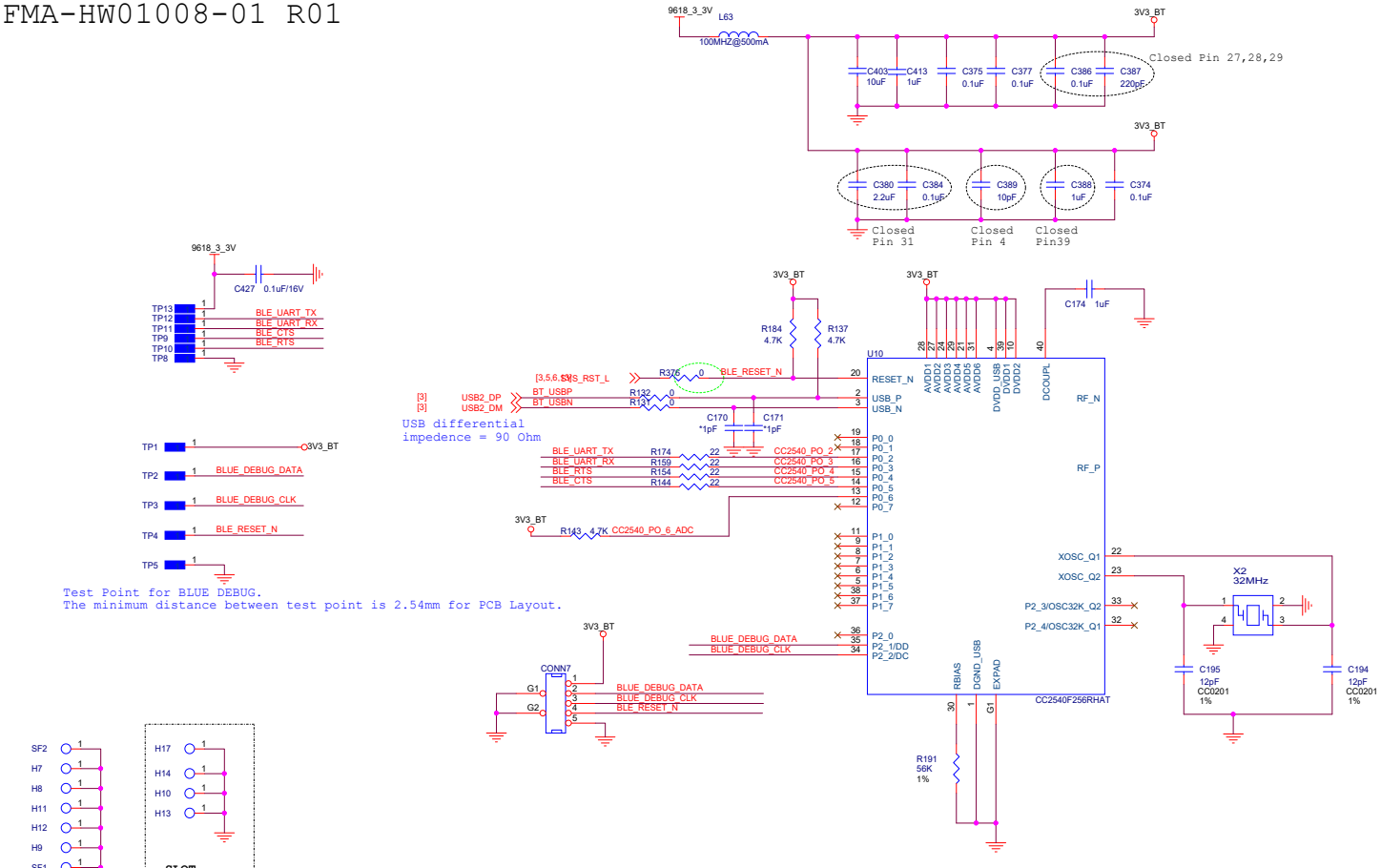
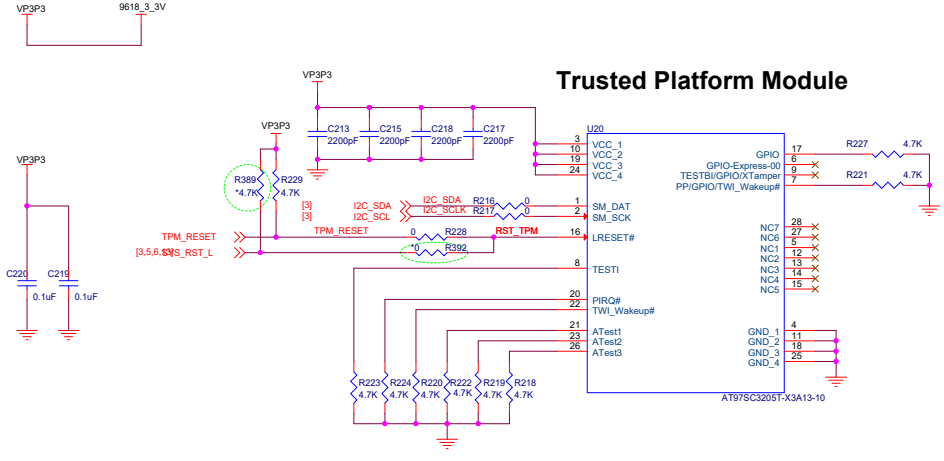


Shielding Slot

Trusted Platform Module



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