FMB100 User manual

Ver.1.1

Oct. 1, 2021

Release Record

Version	Release Date	Comments
0.9	Jul. 1, 2021	Draft release.
1.0	Jul. 16, 2021	Modify the pinout according to latest hardware change.
1.1	Oct. 1, 2021	Update recommended PCB footprint, FCC ID, antenna gain, thickness of the module, description of supported Bluetooth profiles, RF performance at the antenna feed point (which means the internal insertion loss of RF filter is counted in) and tape package information, which is not finalized yet.

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Description:

FMB100 is a dual mode class 2 Bluetooth® V5.2 module. It integrates all necessary components including antenna, RF filter, baseband and profile processors into a small formfactor module in half though hole footprint. With its internal multiple processors, it runs a full Bluetooth stack including multiple profiles such as HSP/HFP, A2DP, AVRCP, OPP, SPP, HID, and GATT based BLE profiles. It also supports high quality A2DP codec such as AptX®. Wideband SBC is supported for HFP/AG applications. It supports two MIC cVc which enables super noise depression performance for headset applications.

FMB100 also supports a Flairmesh property GATT based BLE profile called iGate. It can be used to build a SPP like bi-directional raw data channel over BLE to iOS, Android devices.

With its ASCII command-based control interface, fully qualified Bluetooth stack and modular approvals for major markets such as FCC/CE, it helps customer to integrate Bluetooth functionality to their host system with least efforts.

Typical Bluetooth audio applications:

- Headset
- Industry and office equipment
- Home entertainment and fitness equipment
- Mobile accessories

Features:

- Dual mode Bluetooth® v5.2
- Support BLE 2M PHY
- 11.35dBm BR TX power, -95dBm BR RX sensitivity
- 3.04dBm BLE TX power, -98dBm BLE 1Mb/s -95dBm BLE 2Mb/s RX sensitivity
- Support Profiles: SPP/HID/OPP/iGate supported by standard firmware, HSP/HFP, A2DP, AVRCP, iAP over Bluetooth for Apple, GATT based standard BLE profiles such as HOGP can be supported by special firmware.
- UART/I2C/SPI master multiplexed with PIOs
- 10 digital PIOs (multiplexed with UART/I2C/SPI), 3 LED outputs multiplexed with AIOs
- Support SBC, AAC and AptX codec
- 22mm x 12mm x 2.2mm
- Weight: approximately 1g
- SMT pads for easy and reliable PCB mounting
- QDID: TBD
- FCC ID: 2A22WFMB100
- IC: TBD
- CE
- RoHS compliant

Ordering Number	Package	Items in One Package	Comments
FMB100	Tape	TBD	

Table 1: Ordering Information

Please also supply the customer firmware code issued by Flairmesh Technologies when you place the order.

1 Pinout and Description

1.1 Pin Assignments

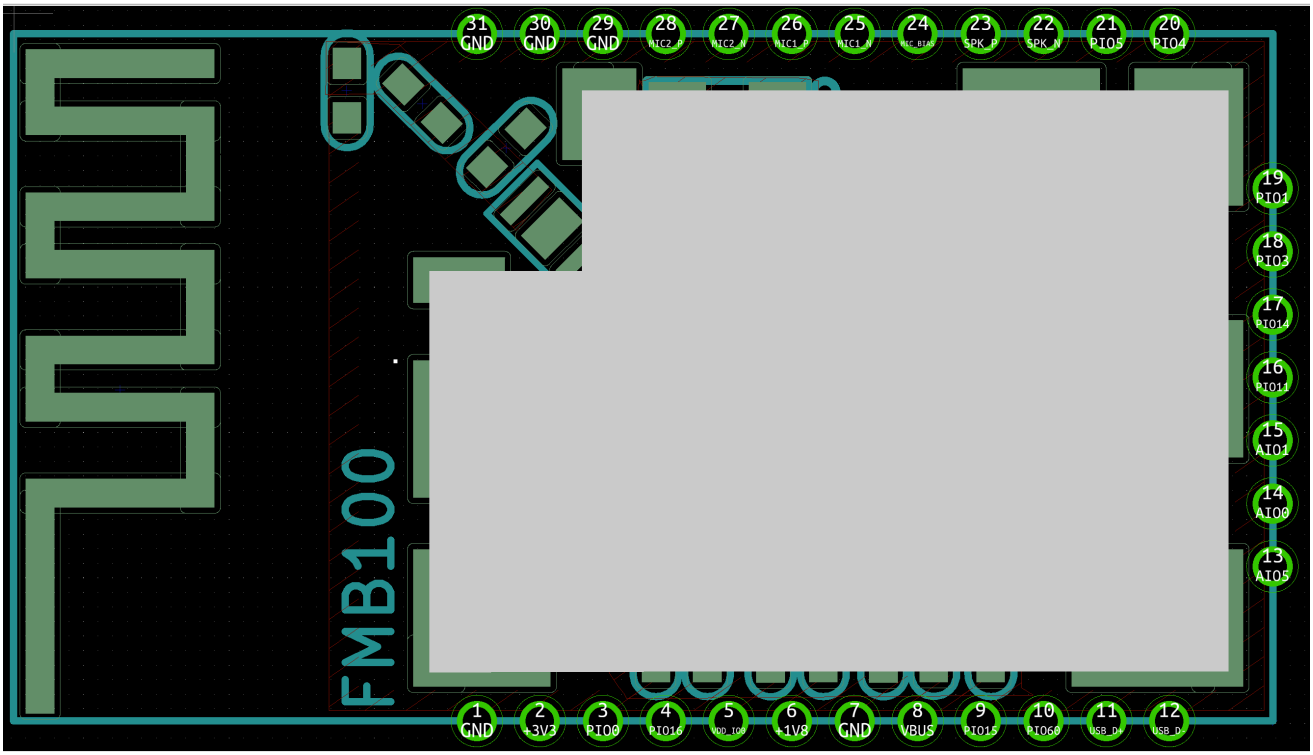

Figure 1: Pinout of FMB100

1.2 Pinout Descriptions

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	3V3/VBAT	Power input	Battery voltage input
3	PIO0/VREG_EN	Digital input	Typically connected to an ON/OFF push button. If power is present from the battery and/or charger, and software has placed the device in the OFF or DORMANT state, a button press boots the device. Also usable as a digital input in normal operation. No pull. Additional function: ■ PIO[0] input only
4	PIO16	Digital bidirectional with programable	Programmable IO 16, weak pull

		strength internal pull-up/pull-down	down when reset
5	VCC_IO	Power input	1.8V/3.3V PIO supply
6	1V8_OUT	Power output	Not recommend for powering external circuits
7	GND	Ground	Ground
8	VCHG	Power input	5V charger input
9	PIO15	Digital bidirectional with programable strength internal pull-up/pull-down	Programmable IO 15, weak pull down when reset
10	PIO60	Input with strong pull-up	Programmable IO 60, weak pull down when reset
11	USB_DP	Digital	USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection
12	USB_DN	Digital	USB Full Speed device D- I/O. IEC-61000-4-2 (device level) ESD Protection
13	AIO5/LED5	Analog or digital input/open drain output	General purpose analog/digital input or open drain LED output 5
14	AIO0/LED0	Analog or digital input/open drain output	General purpose analog/digital input or open drain LED output 0
15	AIO1/LED1	Analog or digital input/open drain output	General purpose analog/digital input or open drain LED output 1
16	PIO11	Digital bidirectional with programable strength internal pull-up/pull-down	Programmable IO 11, strong pull up when reset
17	PIO14	Digital bidirectional with programable strength internal pull-up/pull-down	Programmable IO 14, strong pull up when reset
18	PIO3	Digital bidirectional with programable strength internal pull-up/pull-down	Programmable IO 8, weak pull down when reset
19	PIO1/RESETB	Digital bidirectional with programable strength internal pull-up/pull-down	Automatically defaults to RESETB mode when the device is unpowered, or in off modes. Reconfigurable as a PIO after boot, strong pull up when reset, Alternative function: ■ Programmable I/O line 1
20	PIO4/UART_RX	Digital bidirectional with programable strength internal pull-up/pull-down	Programmable IO 4, weak pull down when resetting, Additional function: ■ UART RX

21	PIO5/UART_TX	Digital bidirectional with programable strength internal pull-up/pull-down	Programmable IO 3, strong pull up when reset, Additional function: ■ UART TX
22	SPK_N	Analog	Headphone/speaker differential output, negative
23	SPK_P	Analog	Headphone/speaker differential output, positive
24	MIC_BIAS	Mic bias output	Mic bias output
25	MIC1_N	Analog	Microphone differential 1 input, negative
26	MIC1_P	Analog	Microphone differential 1 input, positive
27	MIC2_N	Analog	Microphone differential 2 input, negative
28	MIC2_P	Analog	Microphone differential 2 input, positive
29	GND/MIC_GND	Microphone ground	Ground of microphone
30	GND	Ground	Ground
31	GND	Ground	Ground

Table 2: Pinout Definitions

2 Electrical Characteristics

2.1 Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+85	°C
VCHG Voltage	-0.4	7.0	V
USB_DP/USB_DN Voltage	-0.4	3.8	V
VBAT Voltage	-0.4	4.8	V
PIO Voltage	-0.4	3.8	V
LED Voltage	-0.4	7.0	V
AIO Voltage	-0.4	2.1	V

Table 3: Absolute Maximum Rating

2.2 Recommended Operating Conditions

Operating Condition	Min	Typ	Max	Unit
Operating Temperature Range*	-40	--	+85	°C
VCHG	4.75	5.0	6.5	V
USB_DP/USB_DN Voltage	0	--	3.6	V
VBAT Voltage	2.8	3.7	4.6	V
PIO Voltage	1.7	3.3	3.6	V
LED voltage	0	--	6.5	V
AIO Voltage	0	--	1.95	V

Table 4: Recommended Operating Conditions

Note *: Charger operates in a range from -10 to +85 (not including battery).

2.3 Input/output Terminal Characteristics

2.3.1 Digital Terminals

Supply Voltage Levels	Min	Typ	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low	0	-	0.22 x VCC_PIO	V
V_{IH} input logic level high	0.7 x VCC_PIO	-	-	V
Drive current (configurable 2,4,8,12mA)	2	4	12	mA
Output Voltage Levels				
V_{OL} output logic level low, at max rated drive	-	-	0.22 x VCC_PIO	V
V_{OH} output logic level high, at max rated drive	0.75 x VCC_PIO	-	-	V
Pull Strength				
Strong pull-up/down	15	65	150	kΩ
Weak pull-up/down	500	2200	5000	kΩ

Table 5: Digital Terminal

2.3.2 LED Driver Pads

LED driver pads		Min	Typ	Max	Unit
Open drain current	High impedance state	-	-	5	uA
	Current sink state	-	-	50	mA
LED pad resistance	V < 0.5V	-	-	12	Ω
V_{IL} input logic level low		-	-	0.4	V
V_{IH} input logic level high		1.0	-	-	V

Table 6: LED Driver Pads

2.3.3 10-bit Auxiliary ADC

10-bit auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Internal voltage reference		1.746	1.800	1.854	V
Functional input voltage range		0	-	Internal voltage reference	V
Accuracy (Guaranteed monotonic)	INL	-3	-	3	LSB
	DNL	-1	-	2	LSB
Offset		-1	-	1	LSB
Gain error		-1	-	1	%
Hardware conversion time		-	10	-	us
LED pad leakage		-1	-	1	uA
External pad capacitance for < 0.5 LSB error		0	100	-	nF

Table 7: LED Driver Pads

2.3.4 Class-D DAC Audio Output

Parameter	Conditions	Min	Typ	Max	Unit
Input Sample Width	-	-	-	24	Bits
Input Sample Rate, F_{sample}	-	8	-	192	kHz
Output Power	0 dBFS, 32Ω load -3dBFS, 16 Ω load	-	-	30	mW
Load	-	16	32	30k	Ω

Signal to Noise Ratio, SNR	f_{in}=1kHz 48kHz F_{sample} B/W=20Hz->20kHz A-Weighted 0dBFS signal 32Ω load	-	99.3	-	dBA
THD+N	f_{in}=1kHz 48kHz F_{sample} B/W=20Hz->20kHz -1dBFS signal 32Ω load	-	93.5	-	dB
Digital Gain	Digital Gain Resolution = 1/32	-24	-	21.5	dB
Max capacitive load	Per terminal to ground	-	-	100	pF

Table 8: Class-D DAC Audio Output

2.3.5 Class-AB DAC Audio Output

Parameter	Conditions	Min	Typ	Max	Unit
Input Sample Width	-	-	-	24	Bits
Input Sample Rate, F_{sample}	-	8	-	192	kHz
Output Power	0 dBFS, 32Ω load -3dBFS, 16 Ω load	-	-	30	mW
Load	-	16	32	30k	Ω
Signal to Noise Ratio, SNR	f_{in}=1kHz 48kHz F_{sample} B/W=20Hz->20kHz A-Weighted 0dBFS signal 32Ω load	-	100.9	-	dBA
THD+N	f_{in}=1kHz 48kHz F_{sample} B/W=20Hz->20kHz -1dBFS signal 32Ω load	-	93.5	-	dB
Digital Gain	Digital Gain Resolution = 1/32	-24	-	21.5	dB

Table 9: Class-AB DAC Audio Output

2.3.6 High-quality (HQADC) Single-ended Audio Input

Parameter	Conditions	Min	Typ	Max	Unit
Output Sample Width	-	-	-	24	Bits
Output Sample Rate, F_{sample}	-	8	-	96	kHz
Input level	-	-	-	2.4	V pk-pk

Input impedance	0dB to 24dB analog gain	-	20	-	k Ω
	27dB to 39dB analog gain	-	10	-	k Ω
Signal to Noise Ratio, SNR	f_{in}=1kHz 48kHz F_{sample} B/W=20Hz->20kHz A-Weighted THD+N < 0.1% 2.4V pk-pk input (0dB gain)	-	101.1	-	dBA
THD+N	f_{in}=1kHz 48kHz 2.4V pk-pk input (0dB gain)	-	85.9	-	dB
Digital Gain	Digital Gain Resolution = 1/32	-24	-	21.5	dB
Analog Gain	3dB Steps	0	-	39	dB

Table 10: High-quality Single Ended Audio Input

2.3.7 High-quality (HQADC) Differential Audio Input

Parameter	Conditions	Min	Typ	Max	Unit
Output Sample Width	-	-	-	24	Bits
Output Sample Rate, F_{sample}	-	8	-	96	kHz
Input level	-	-	-	2.4	V pk-pk
Input impedance	0dB to 24dB analog gain	-	20	-	k Ω
	27dB to 39dB analog gain	-	10	-	k Ω
Signal to Noise Ratio, SNR	f_{in}=1kHz 48kHz F_{sample} B/W=20Hz->20kHz A-Weighted THD+N < 0.1% 2.4V pk-pk input (0dB gain)	-	99.4	-	dBA
THD+N	f_{in}=1kHz 48kHz 2.4V pk-pk input (0dB gain)	-	95.5	-	dB
Digital Gain	Digital Gain Resolution = 1/32	-24	-	21.5	dB
Analog Gain	3dB Steps	0	-	39	dB

Table 11: Class-D DAC Audio Output

2.3.8 Microphone Bias

Parameter	Conditions	Min	Typ	Max	Unit
Output voltage (Tunable, step = 0.1V)	-	1.5	-	2.1	V

Output current capability	-	0.07	-	3.00	mA
Output noise	B/W=20Hz->20kHz Unweighted	4.5	5.1	7.3	uVrms
Crosstalk between microphones	Using recommended application circuit	-	80	-	dB
Load capacitance	From parasitic PCB routing and package	-	-	0.1	nF

Table 12: Microphone Bias

2.3.9 VBAT voltage measurement accuracy

Measurement	Min	Typ	Max	Unit
VBAT voltage measurement accuracy	-	+/-1	+/-3	%

Table 13: VBAT Measurement Accuracy

2.4 Power consumptions

Operating Condition	Typical	Unit
Dormant	<20	uA
Deep sleep, idle	50	uA
Connected, 495ms BT Sniff sub-rating	100	uA
Connected, 187ms BT Sniff, 2 links, four slots no retry, AFH on	0.27	mA
Connected, 11.25ms BT Sniff	1.5	mA
Connected with audio streaming (A2DP), SBC in 192 kbit, SBC Out 192kbit, Output Mono LP_DAC 48 KHz	5	mA

Table 14: Power consumptions

Note:

Power consumption depends on the firmware used. Typical values are shown in the table.

Sniff mode ----- In Sniff mode, the duty cycle of the slave's activity in the piconet may be reduced. If a slave is in active mode on an ACL logical transport, it shall listen in every ACL slot to the master traffic, unless that link is being treated as a scatternet link or is absent due to hold mode. With sniff mode, the time slots when a slave is listening are reduced, so it benefits the power consumption of the slave and the master shall only transmit to a slave in specified time slots. The sniff anchor points are spaced regularly with an interval of Tsniff, which depends on the firmware used.

3 Physical Interfaces

3.1 Power Supply

There are two power supply schemes available for the module. It can be powered by a Li-poly battery (3.7V) or a 3.3V DC. Please refer to the reference designs in 5.

3.2 Reset

The module may be reset from several sources: RESETB pin, power-on reset, USB charger attach reset and software configured watchdog timer.
The RSTB pin is an active low reset. It is recommended that RSTB be applied for a period greater than 120us.
At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The pull-down state is shown below.

Pin Name / Group	Pin Status on Reset
USB_DP	Tristate
USB_DN	Tristate
PIO0	No Pull
PIO[1,3,11,14]	PUS
PIO[4,5,16,60]	PDW

Table 15: Pin Status on Reset

Note: PUS – Strong pull-up, PDS – Strong pull-down, PUW – Weak pull-up, PDW – Weak pull-down.

If RSTB is held low for > 1.8 s and VCHG is not applied, the module turns off. A rising edge on PIO0 or VCHG is then required to power on.

3.3 Audio Interfaces

3.3.1 Digital Audio Interface

Audio digital interfaces include:

- Digital microphone inputs
- Standard I²S/PCM interface (Input only)

3.4 General Purpose Analog IO

The module has three general-purpose analogue interface pins multiplexed with LED pads. In a Li-poly

battery application, the VBAT pin can measure the battery voltage directly.

3.5 LED Drivers

The FMB100 includes a 5 PWM LED driver for driving RGB LEDs for producing a wide range of colors. There are 3 open-drain LED outputs multiplexed with AIOs. Any PIOs can also be mapped into LED output by firmware.

3.6 Serial Interfaces

3.6.1 UART

The module has a standard UART serial interface that provides a simple mechanism for communicating using RS232 protocol.

Table 16 : Possible UART Settings

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4M baud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

3.6.2 USB

FMB100 has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices. The USB interface on FMB100 acts as a USB peripheral, responding to requests from a master host controller.
FMB100 contains internal USB termination resistors and requires no external resistors.
FMB100 supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification), supports USB standard charger detection, and fully supports the USB Battery Charging Specification v1.2.
With special firmware FMB100 also supports USB HID/CDC and audio function.

3.6.3 I2C

Any two PIOs can be used to form a master I2C interface.

3.6.4 SPI Interface

Any four PIOs can be used to form a SPI interface. Firmware can be customized to connect with variable peripherals.

4 iNova Stack

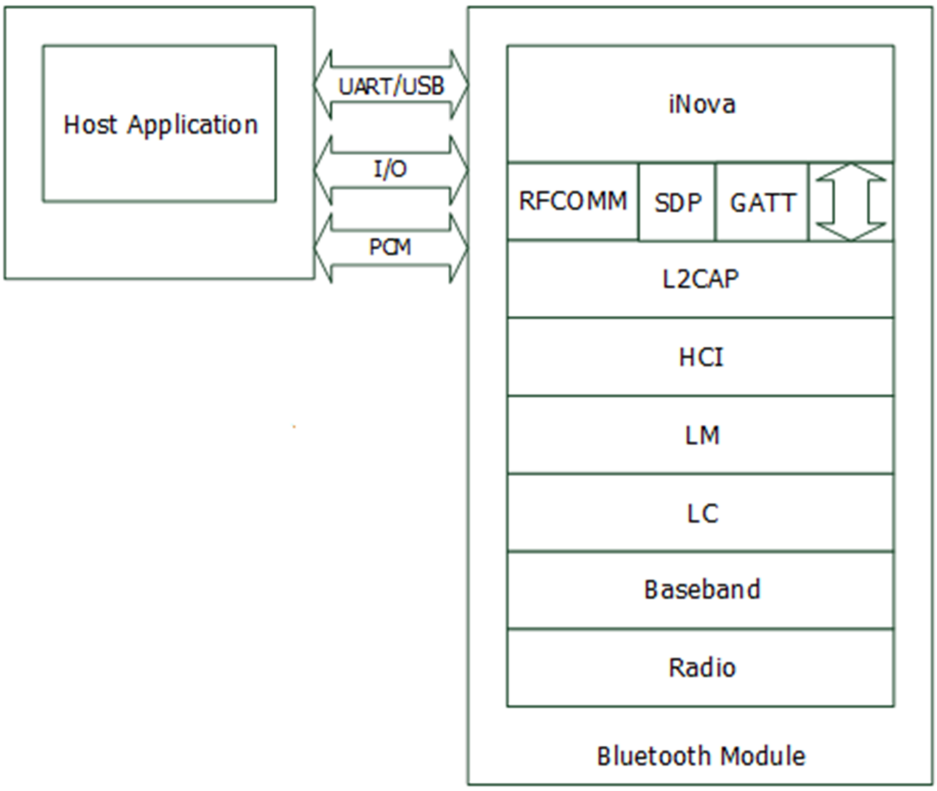

Figure 2: FMB100 Stacks

FMB100 is supplied with Bluetooth 5.2 compliant stack firmware. With Flairmesh's iNova profile stacks, the host MCU can easily integrate HFP, A2DP, AVRCP, SPP, OPP, HID profiles and iAP over Bluetooth functions, it also supports GATT based profiles over BLE such as HOGP.

5 Reference Design

TBD

Figure 3: Schematics reference design

6 Mechanical Size and Recommended PCB Footprint

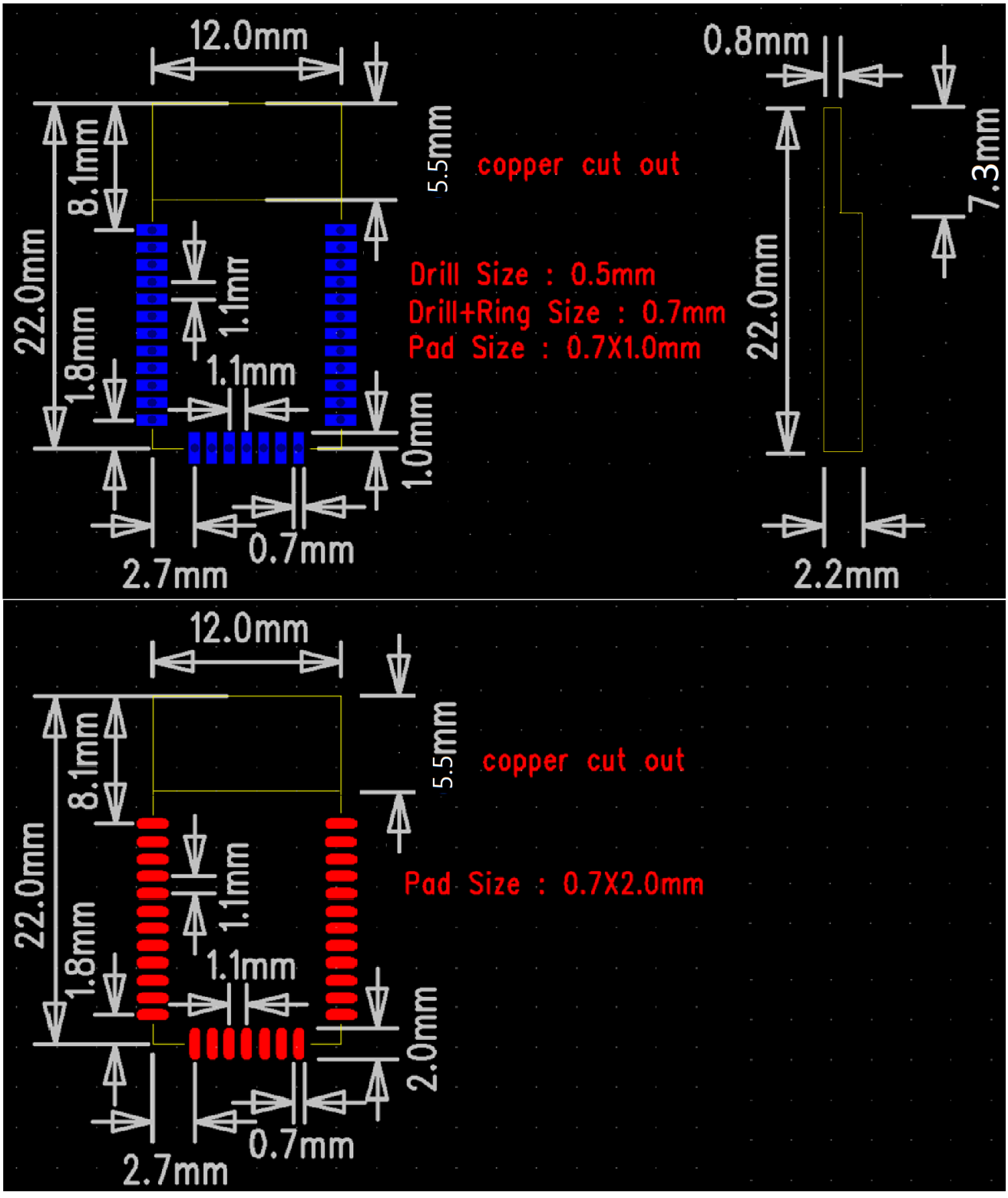

Figure 4: Mechanical Size and Recommended PCB Footprint

7 RF Layout Guidelines

FMB100 integrates an on-board Meander line antenna to radiate and receive the RF signals. The antenna has been well designed and tuned for common usage but it still needs to have good ground clearance around the antenna to get good RF performance.

1. No ground below antenna region (copper cut out in Figure 4) of the FMB100.
2. There should also have a good ground panel and clearance on the main PCB board on which the module is mounted. As shown in Figure 5.

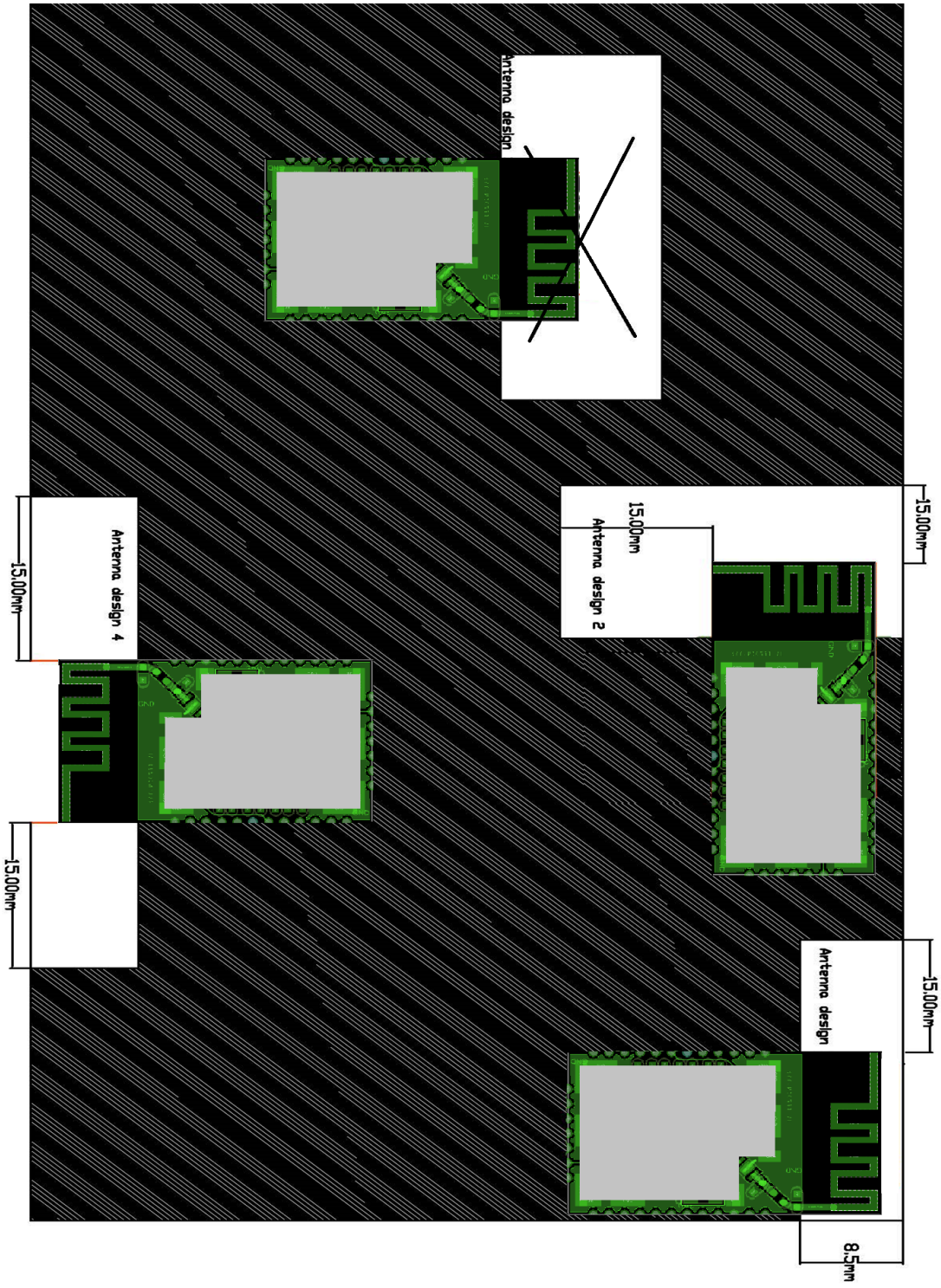

Figure 5 : Placement the module and the ground of main PCB Board

8 Reflow Profile

FMB100 is compatible with industrial standard reflow profile for Pb-free solders. The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow.

There are four zones:

Preheat Zone - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.

Equilibrium Zone - This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.

Reflow Zone- The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.

Cooling Zone - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

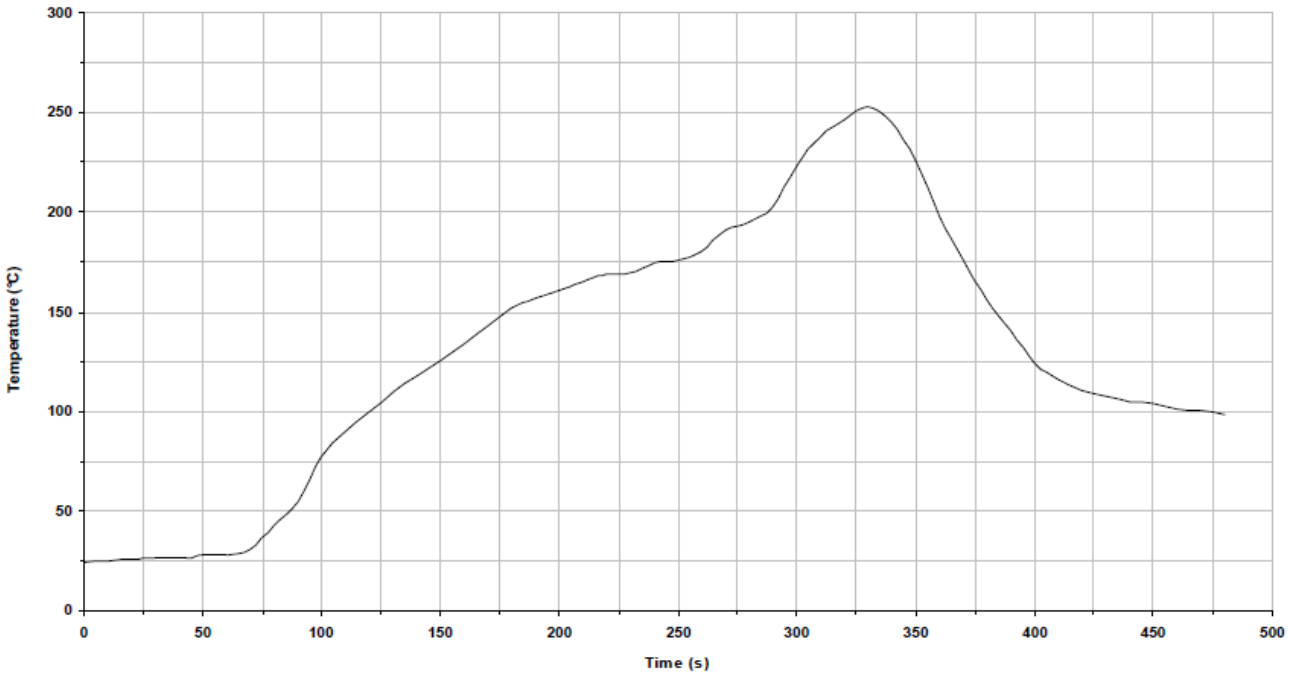

Figure 6: Typical Lead-Free Re-flow Solder Profile for FMB100

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C ±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 255°C

Note: Customer might choose a local 0.2mm thickness solder cream for the module, or use 0.15mm to match other components in the same PCB.

9 Package

TBD

Figure 7: Tape Package

Plastic tape, plus aluminum bags do vacuum packing. Items in One Package number of TBD PCS, external aluminum foil vacuum packaging.

The module's Moisture Sensitivity Level is level 3 in accordance with JEDEC J-STD-020.

l'utilisateur ou des tiers.

Ce dispositif ne doit pas être utilisé à proximité d'une autre antenne ou d'un autre émetteur.

FCC Statement：

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user’ s authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference,and (2) this device must accept any interference received, including interference that may cause undesired operation.

OEM Guidance

1. Applicable FCC rules

This module is granted by Single Modular Approval. It complies to the

requirements of FCC part 15C, section 15.247 rules.

2. The specific operational use conditions

This module can be used in IoT devices. The input voltage to the module is nominally 2.2V-5.5V DC. The operational ambient temperature of the module is -20 to 85 degree C. Only the embedded PCB antenna is allowed. Any other external antenna is prohibited.

3.Limited module procedures

N/A

4.Trace antenna design

N/A

5.RF exposure considerations

The equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment can operated with minimum distance 20cm between the radiator and your body.

6. Antenna

Antenna type :PCB Antenna; Antenna Max. Peak Gain 2.7dBi

7. Label and compliance information

An exterior label on OEM's end product can use wording such as the following: "Contains FCC ID: 2A22WFMB100"

8. Information on test modes and additional testing requirements

a)The modular transmitter has been fully tested by the module grantee on the required number of channels,modulation types, and modes, it should not be necessary for the host installer to re-test all the available transmitter modes or settings. It is recommended that the host product manufacturer, installing the modular transmitter,perform some investigative measurements to confirm that the resulting composite system does not exceed the spurious emissions limits or band edge limits (e.g., where a different antenna may be causing additional emissions).

b)The testing should check for emissions that may occur due to the intermixing of emissions with the other transmitters, digital circuitry, or due to physical properties of the host product (enclosure). This investigation is especially important when integrating multiple modular transmitters where the certification is based on testing each of them in a stand-alone configuration. It is important to note that host product manufacturers should not assume that because the modular transmitter is certified that they do not have any responsibility for final product compliance.

c)If the investigation indicates a compliance concern the host product manufacturer is obligated to mitigate the issue. Host products using a modular transmitter are subject to all the applicable individual technical rules as well as to the general conditions of operation in Sections 15.5, 15.15, and 15.29 to not cause interference. The operator of the host product will be obligated to stop operating the device until the interference have been corrected .

9. Additional testing, Part 15 Sub part B disclaimer The final host / module combination need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The host integrator installing this module into their product must ensure that the final composite product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operation and should refer to guidance in KDB 996369. For host products with certified modular transmitter, the frequency range of investigation of the composite system is specified by rule in Sections 15.33(a)(1) through (a)(3), or the range applicable to the digital device, as shown in Section 15.33(b)(1), whichever is the higher frequency range of investigation When testing the host product, all the transmitters must be operating.The transmitters can be enabled by using publicly-available drivers and turned on, so the transmitters are active. In certain conditions it might be appropriate to use a technology-specific call box (test set) where accessory 50 devices or drivers are not available. When testing for emissions from the unintentional radiator, the transmitter shall be placed in the receive mode or idle mode, if possible. If receive mode only is not possible then, the radio shall be passive (preferred) and/or active scanning. In these cases, this would need to enable activity on the communication BUS (i.e., PCIe, SDIO, USB) to ensure the unintentional radiator circuitry is enabled. Testing laboratories may need to add attenuation or filters depending on the signal strength of any active beacons (if applicable) from the enabled radio(s). See ANSI C63.4, ANSI C63.10 and ANSI C63.26 for further general testing details.
The product under test is set into a link/association with a partnering device, as per the normal intended use of the product. To ease testing, the product under test is set to transmit at a high duty cycle, such as by sending a file or streaming some media content.